

FIG. 1

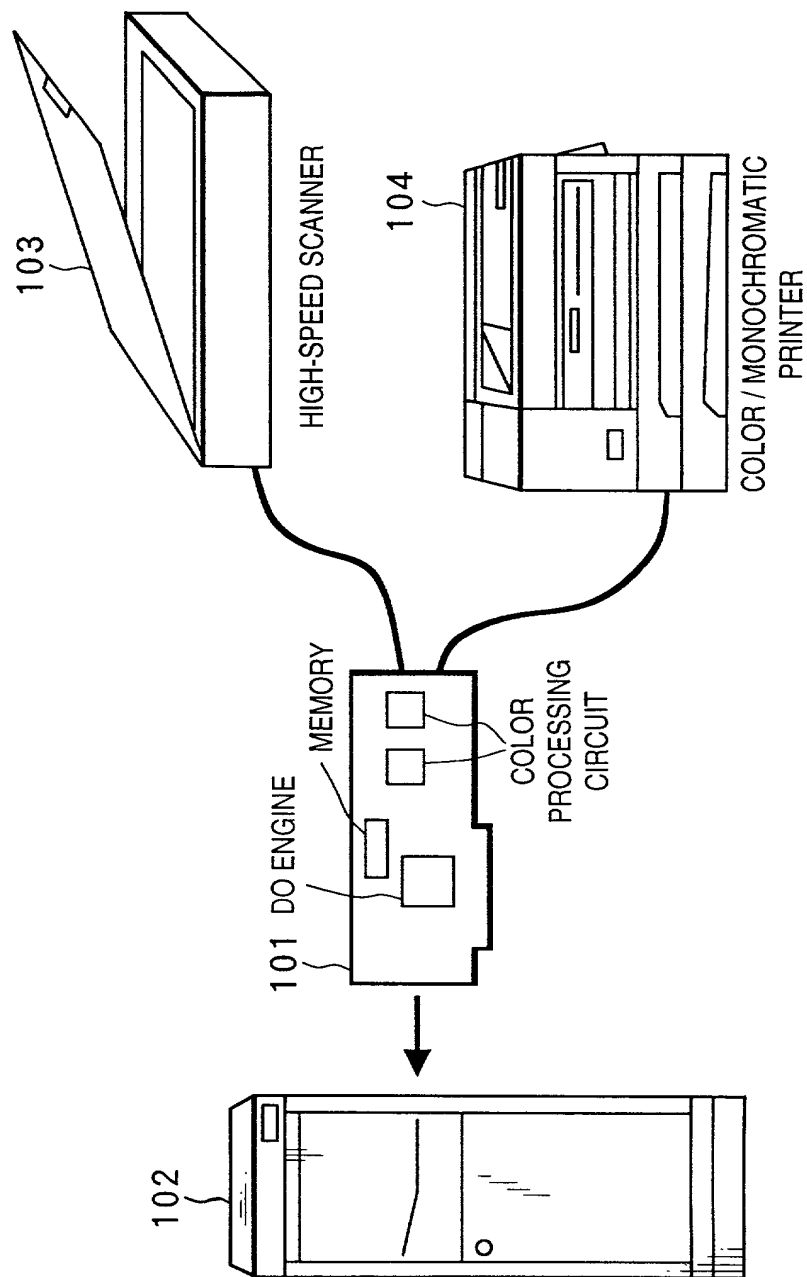


FIG. 2

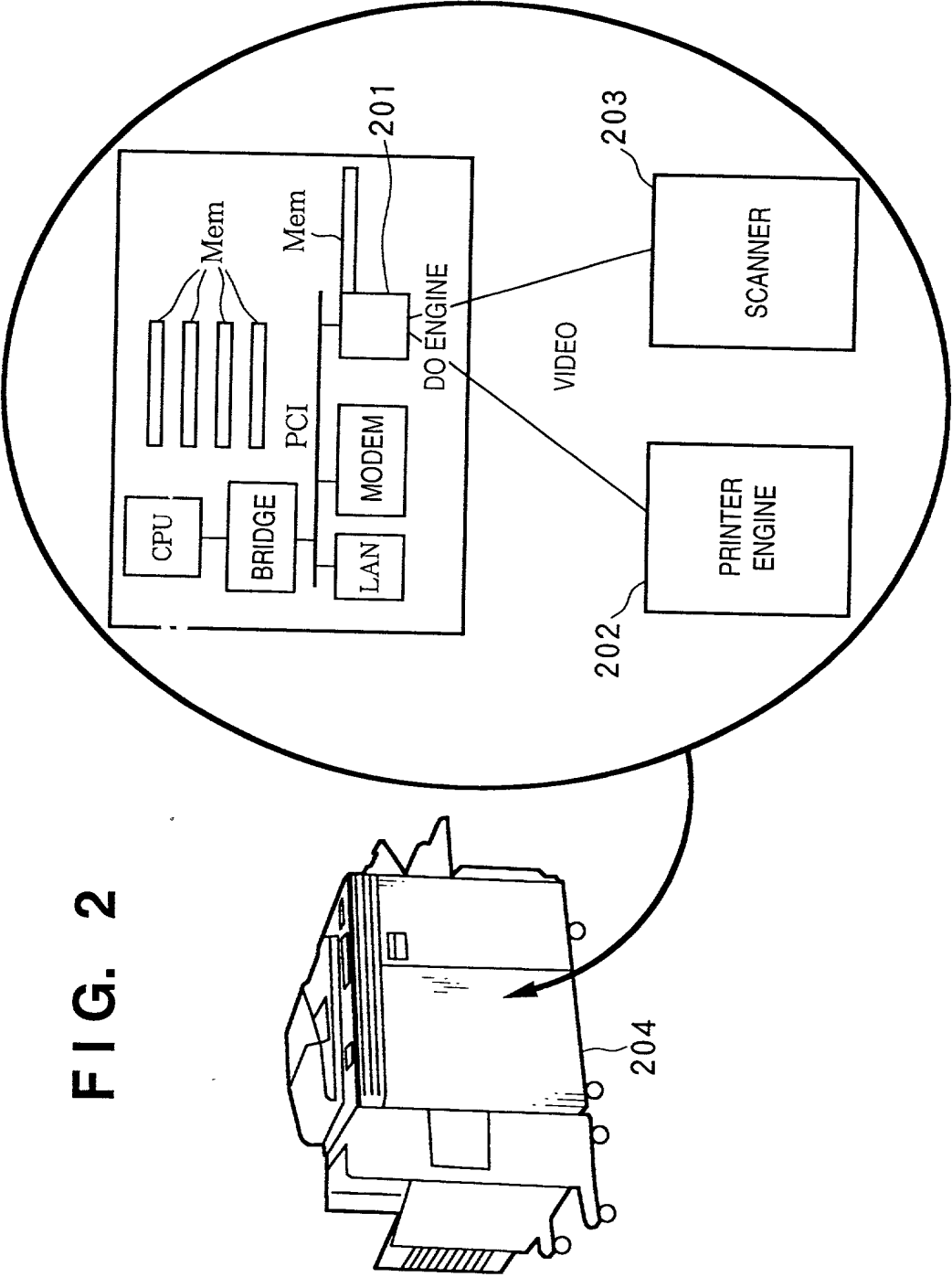


FIG. 3A

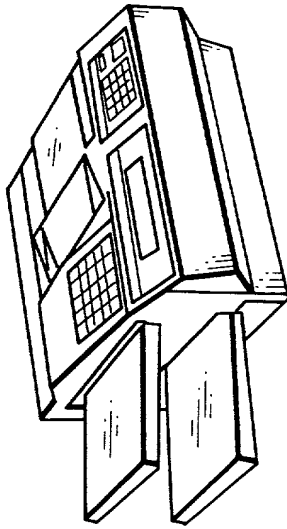


FIG. 3B

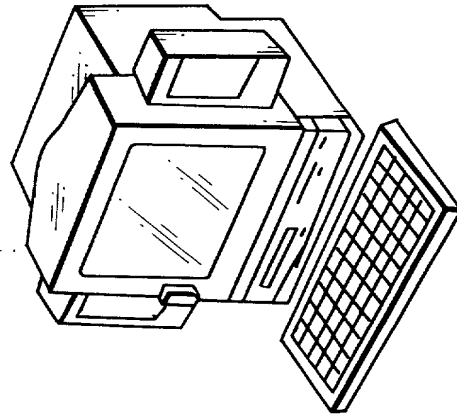
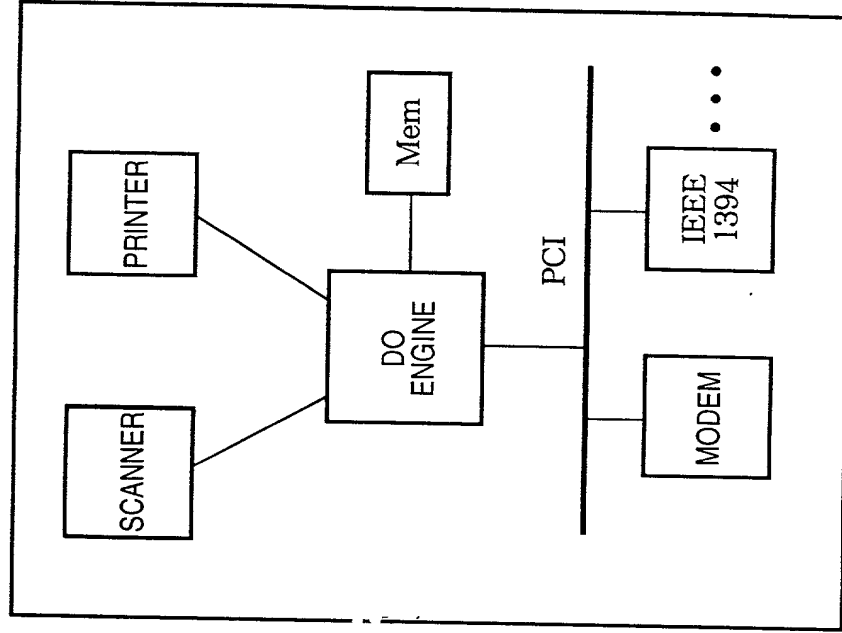


FIG. 3C



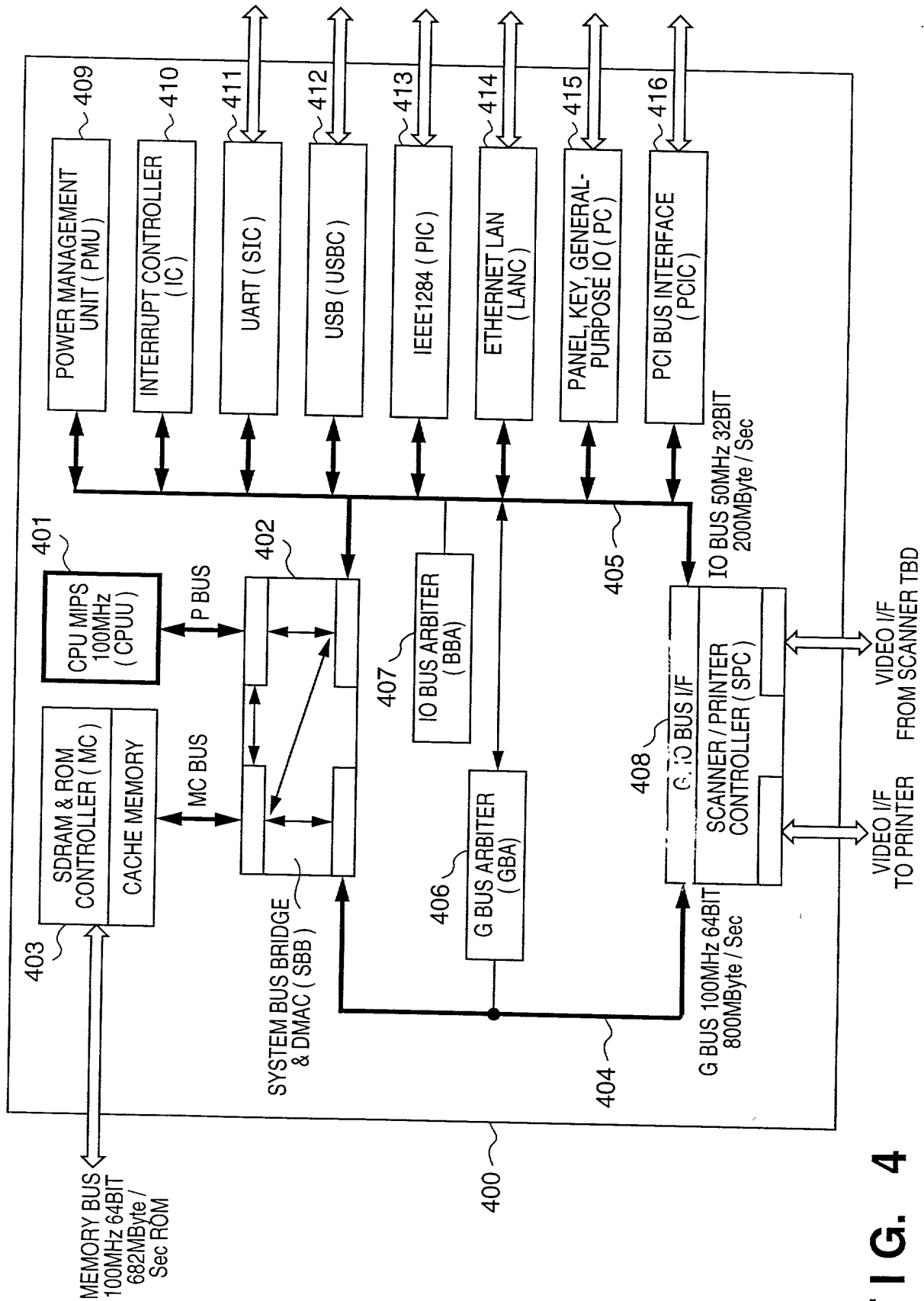


FIG. 5

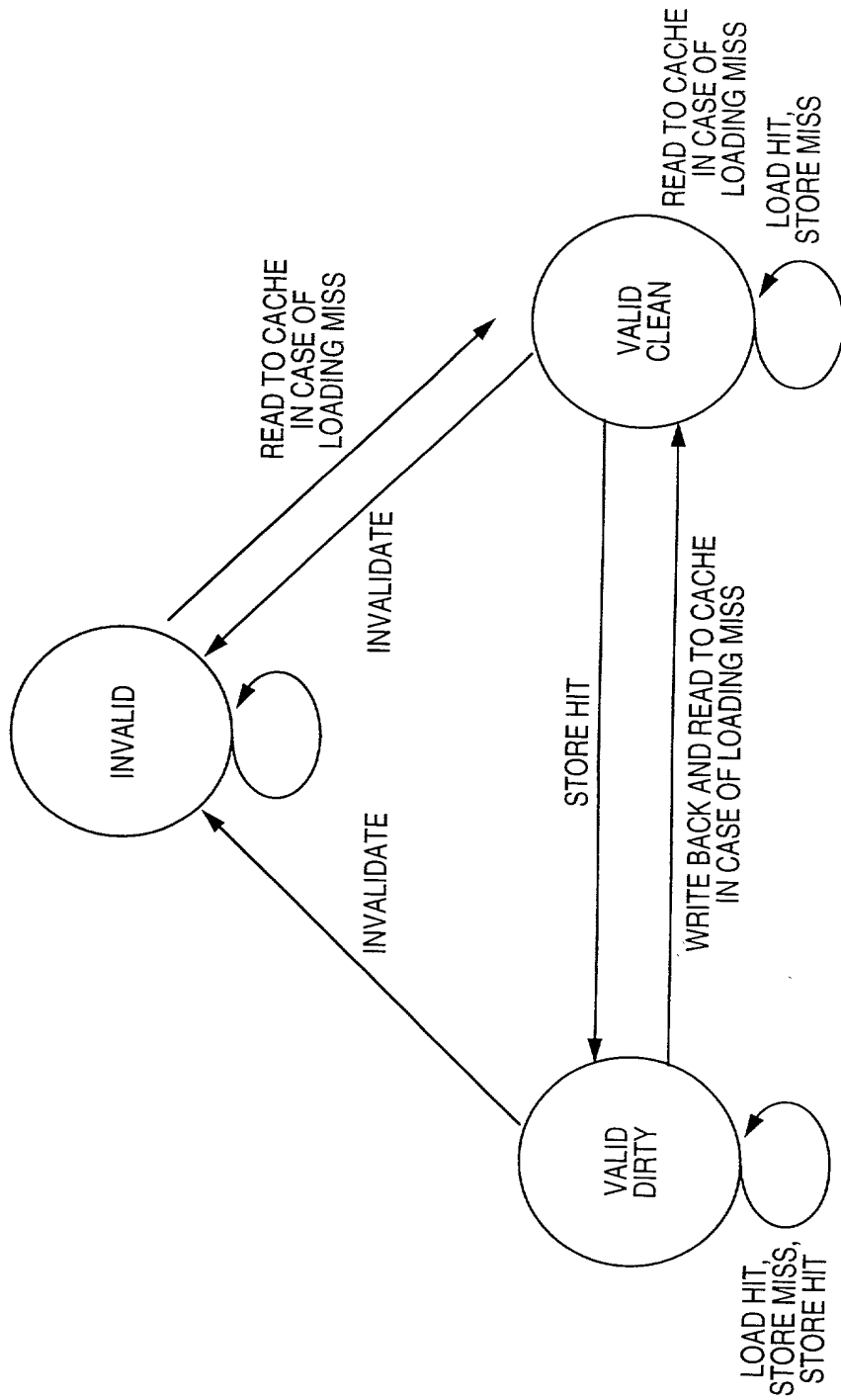


FIG. 6

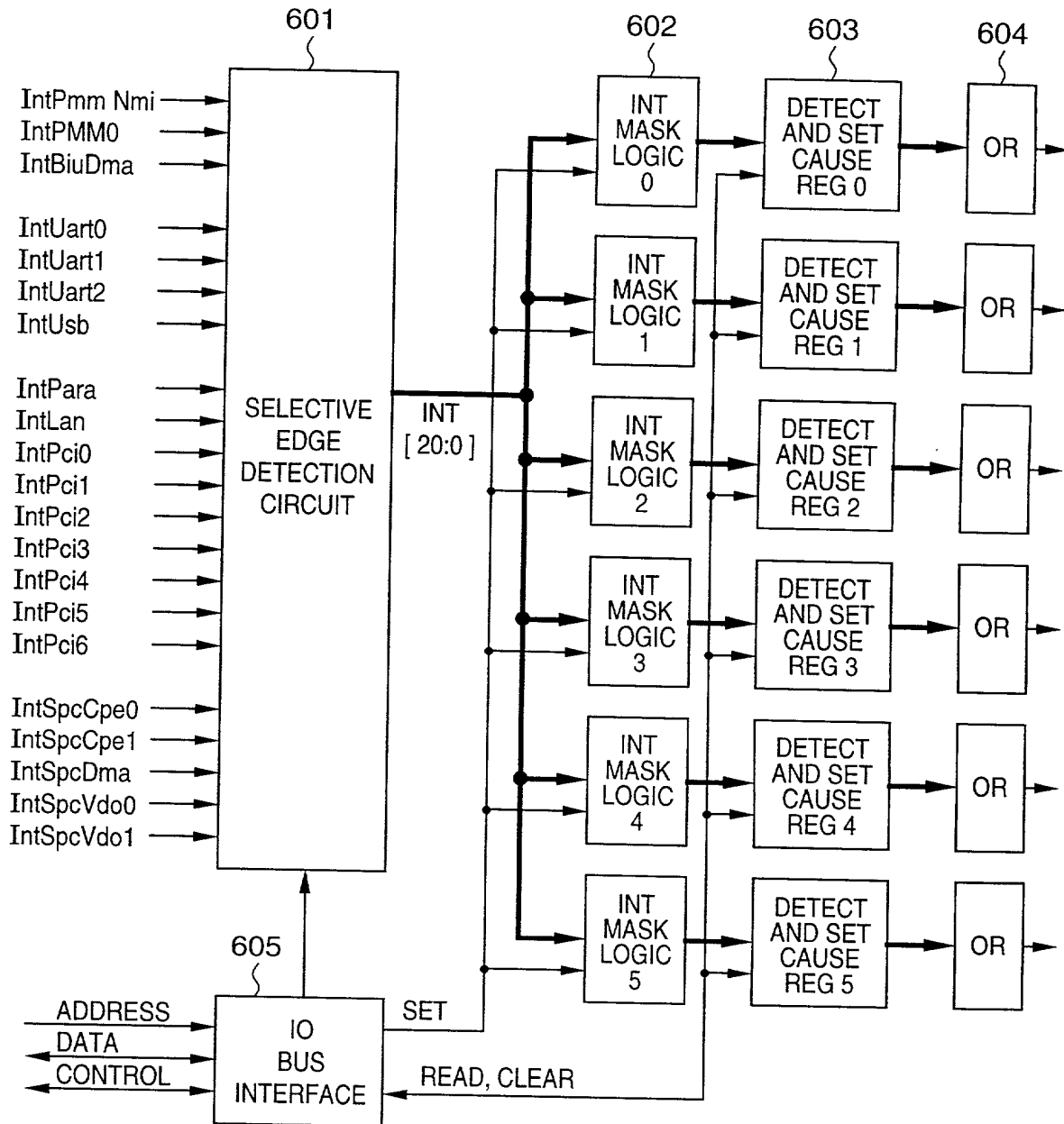
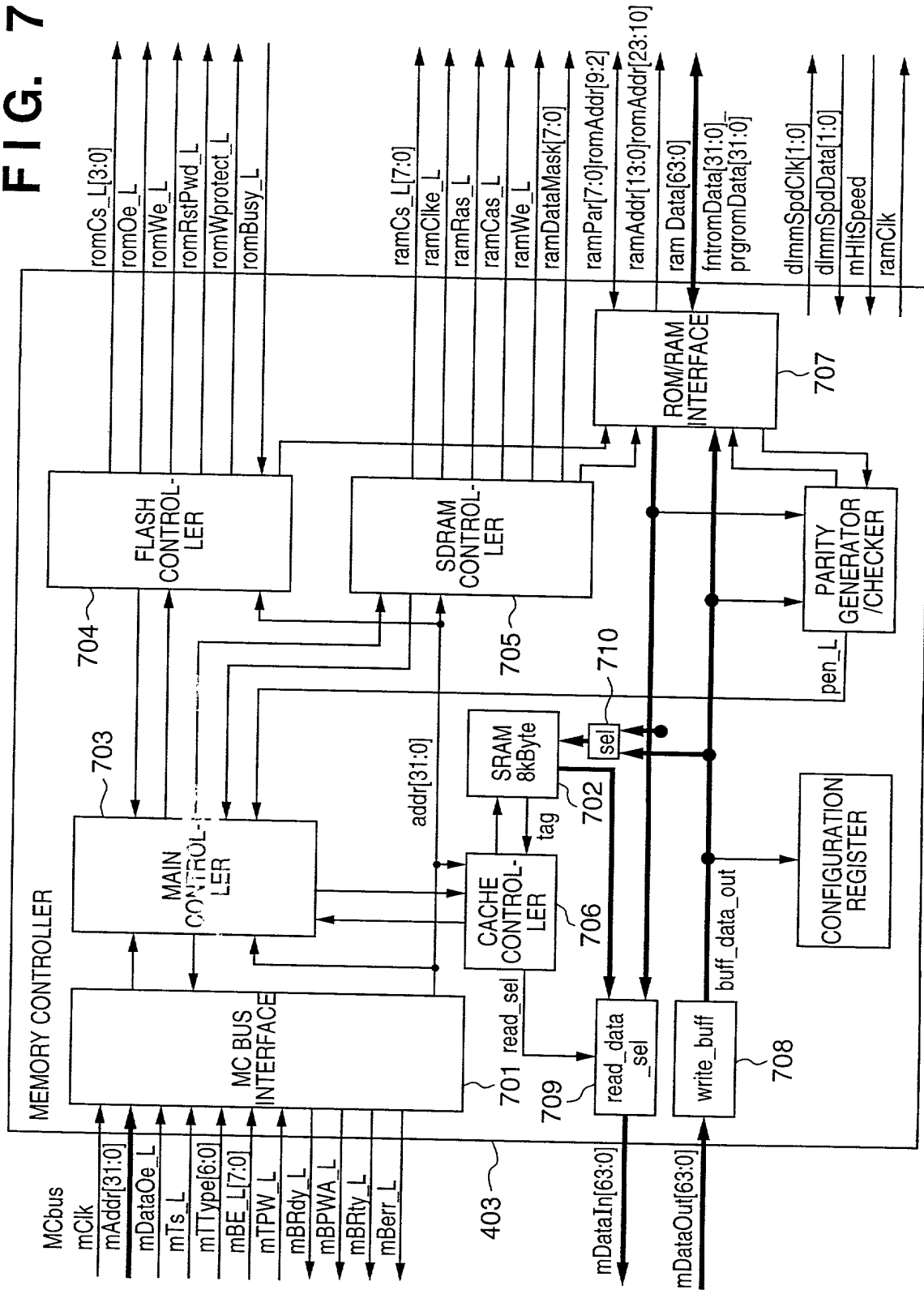


FIG. 7



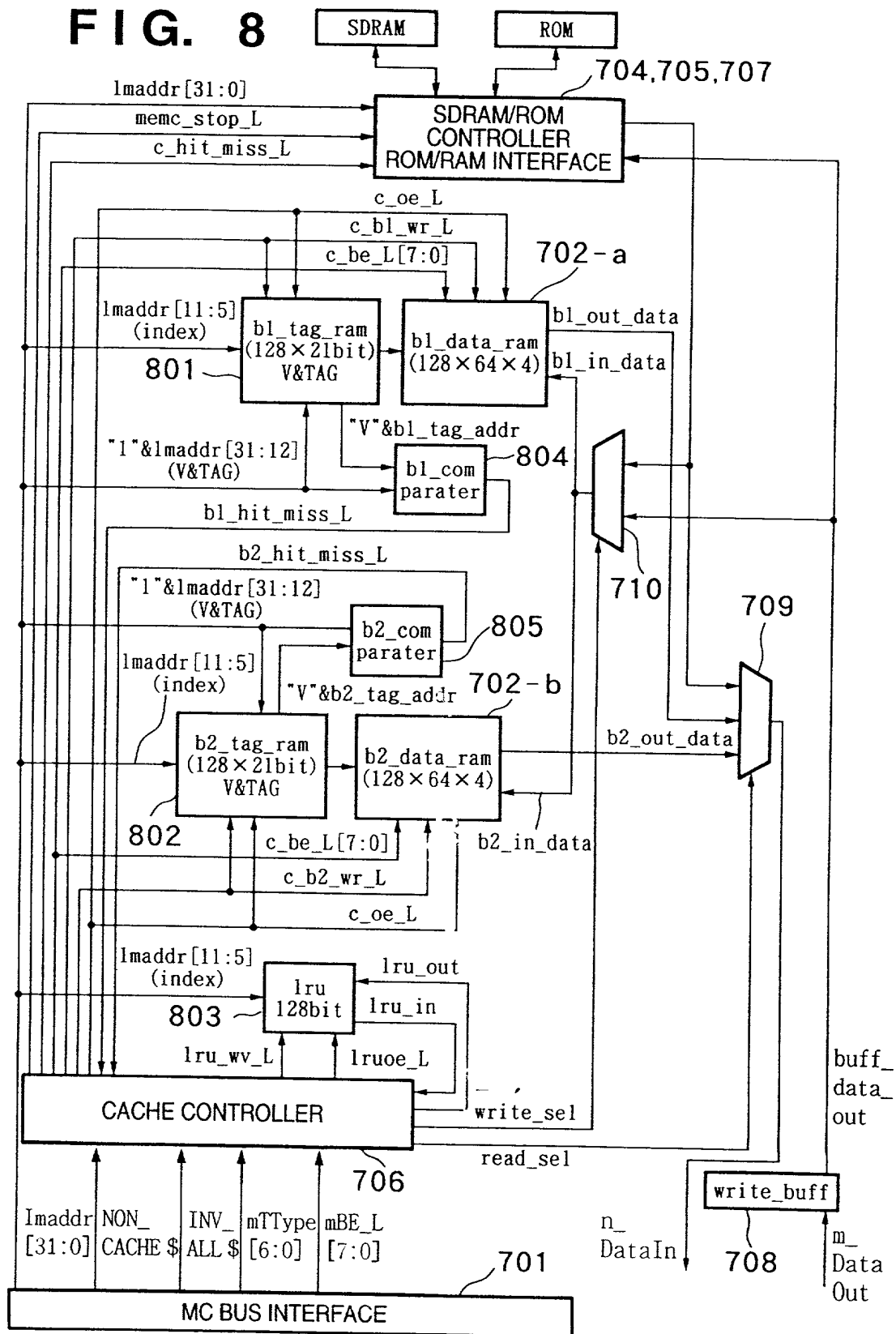
**FIG. 8**



FIG. 9

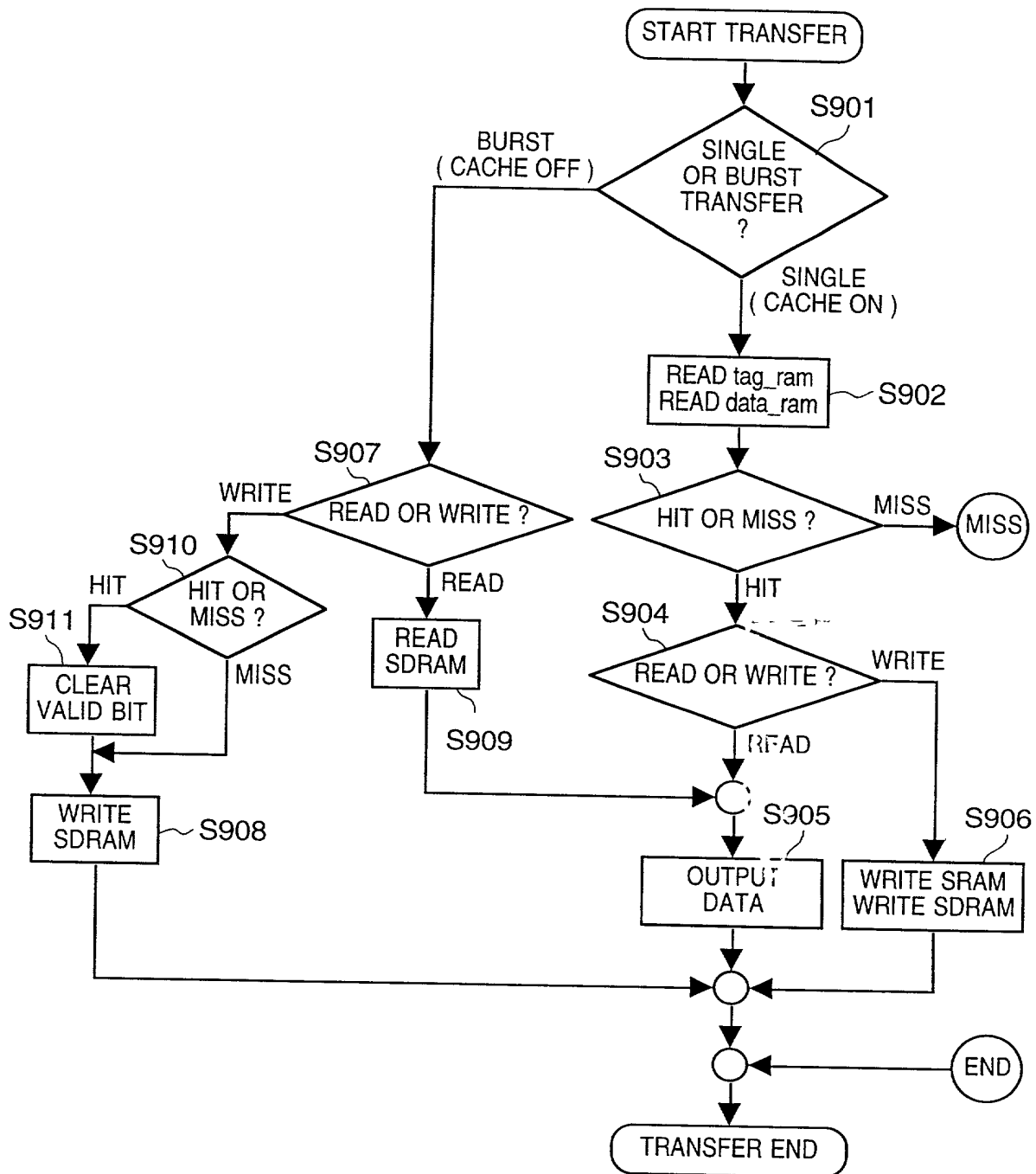


FIG. 10

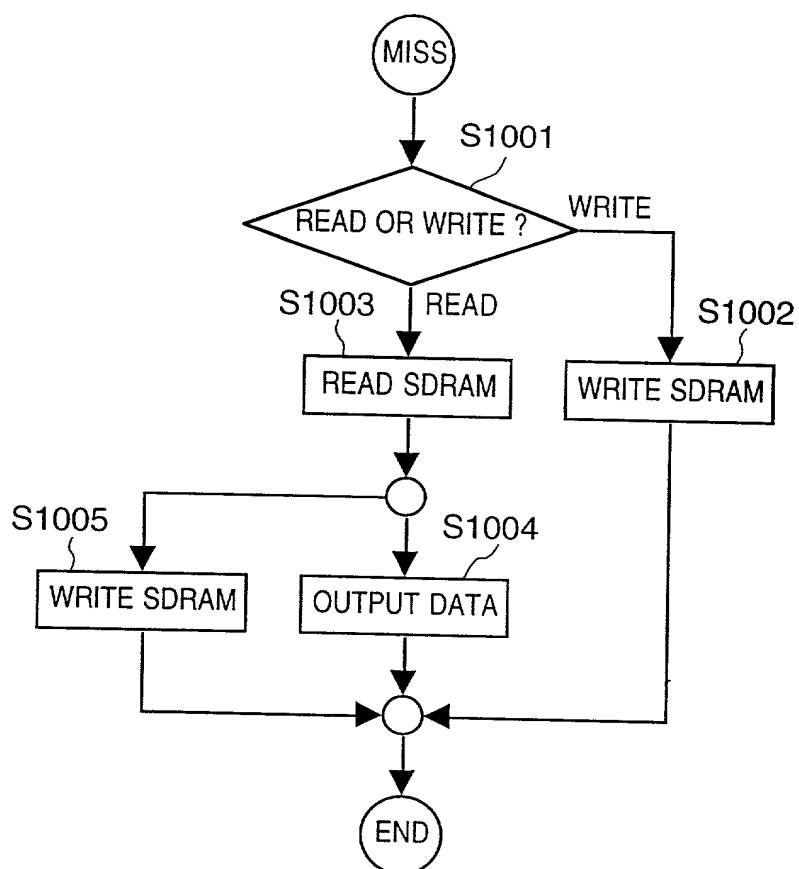
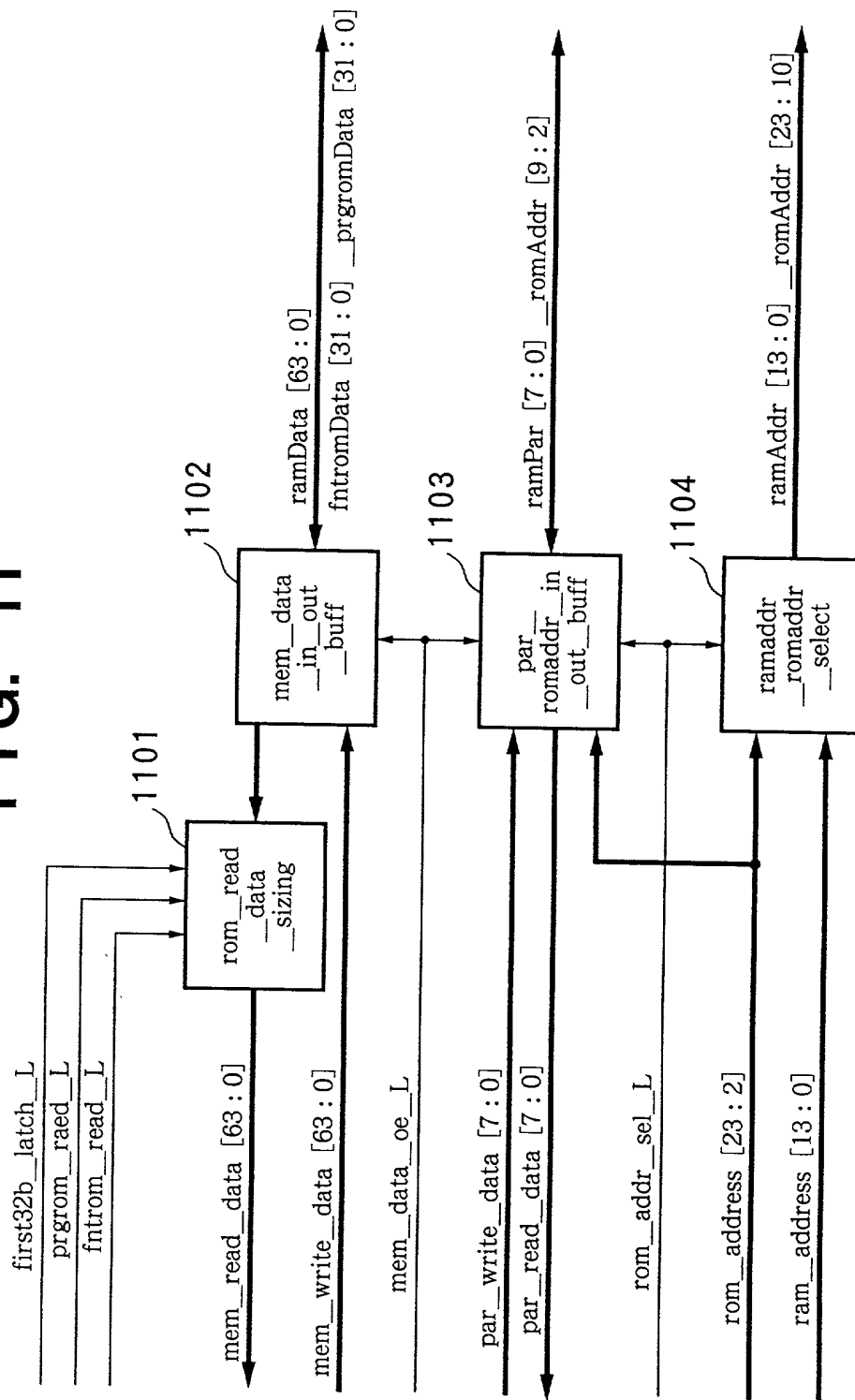
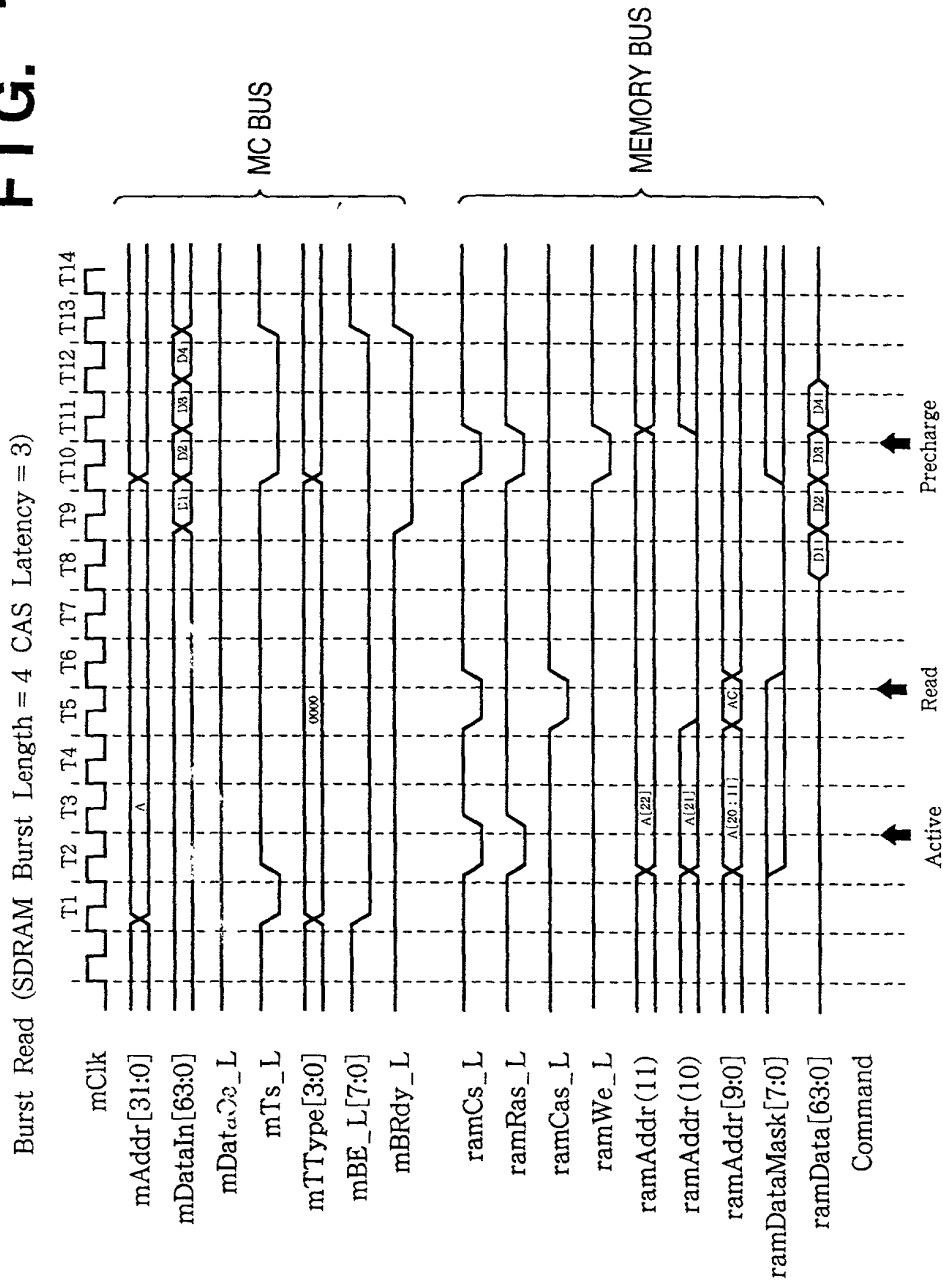
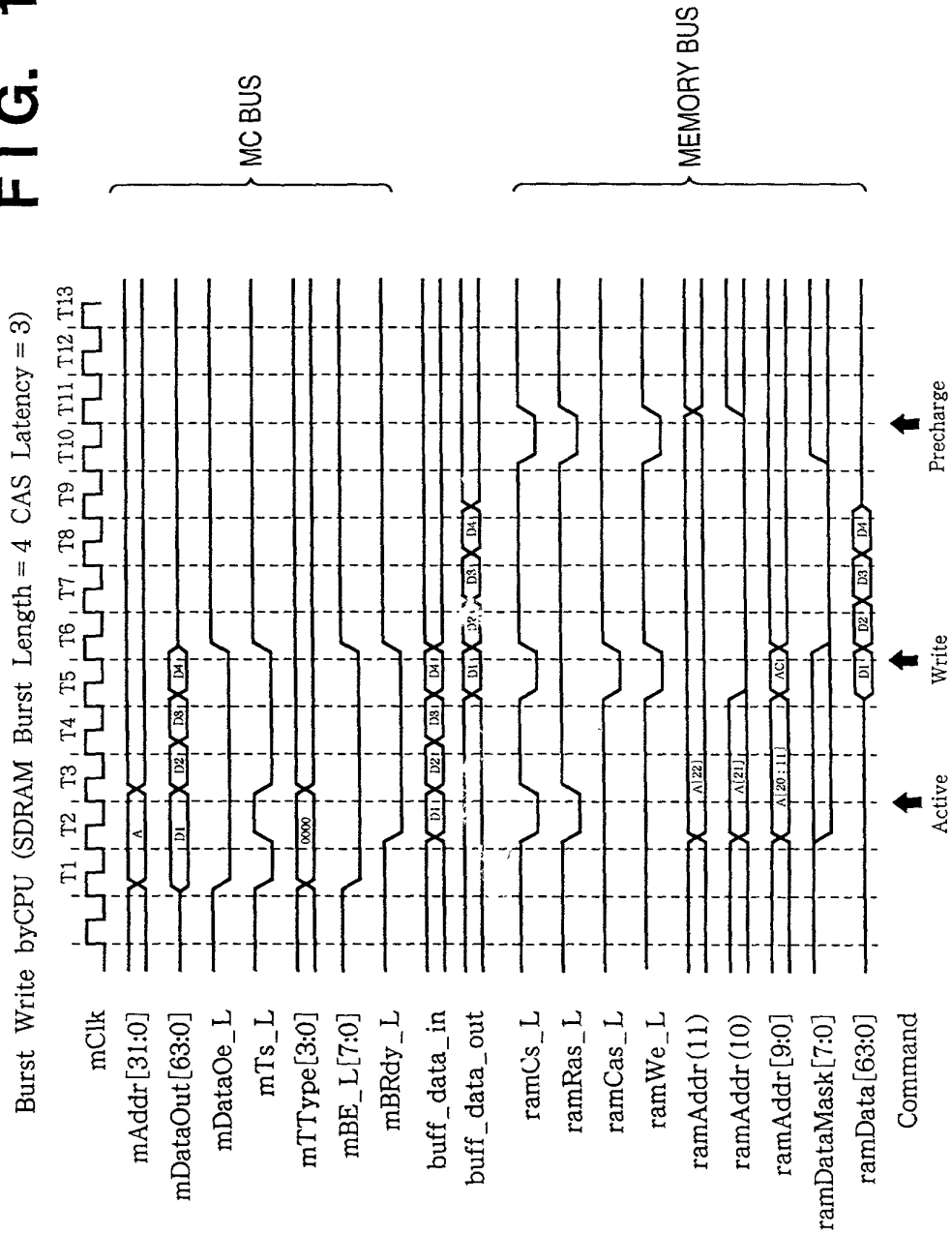


FIG. 11



**FIG. 12**

**FIG. 13**

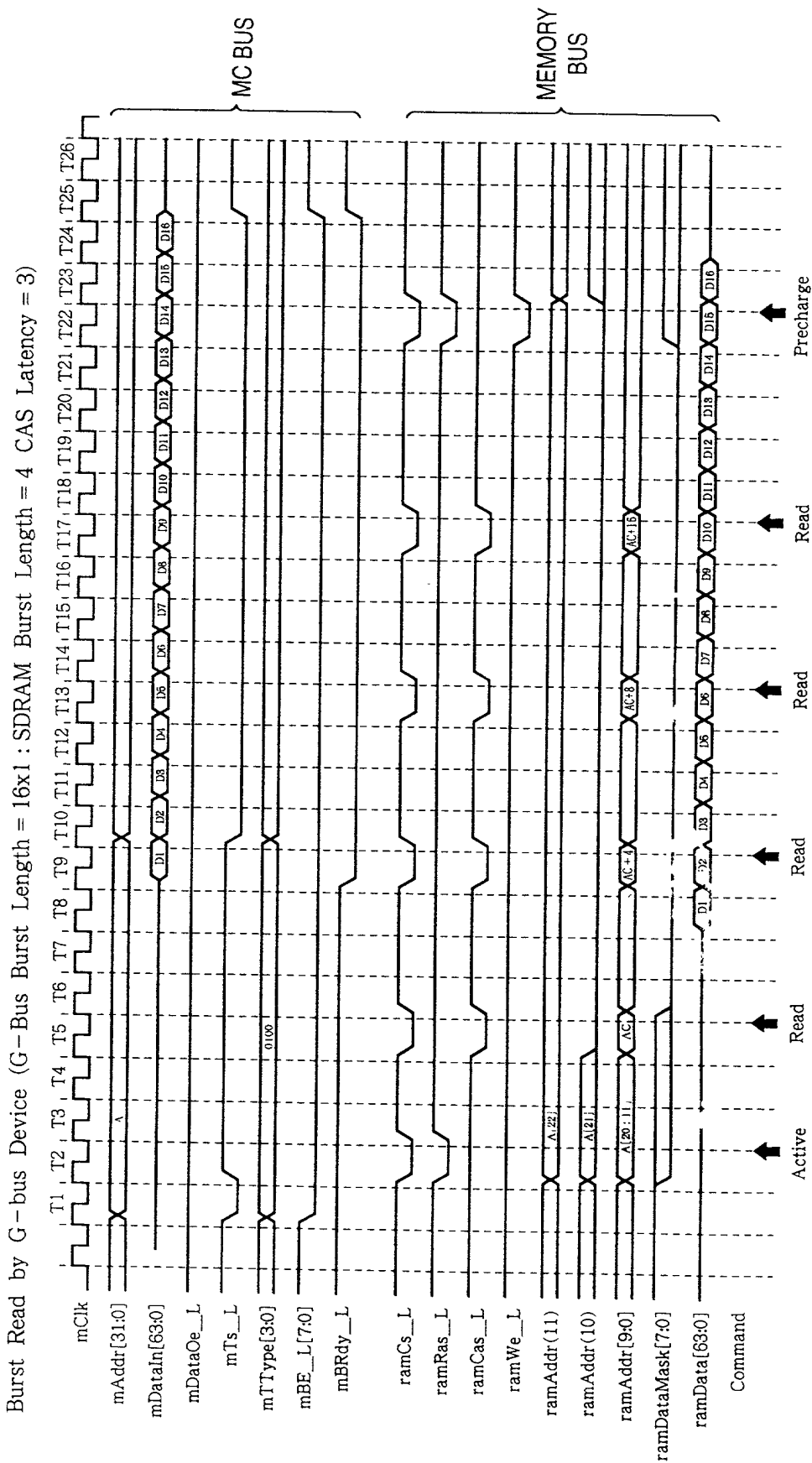


FIG. 14

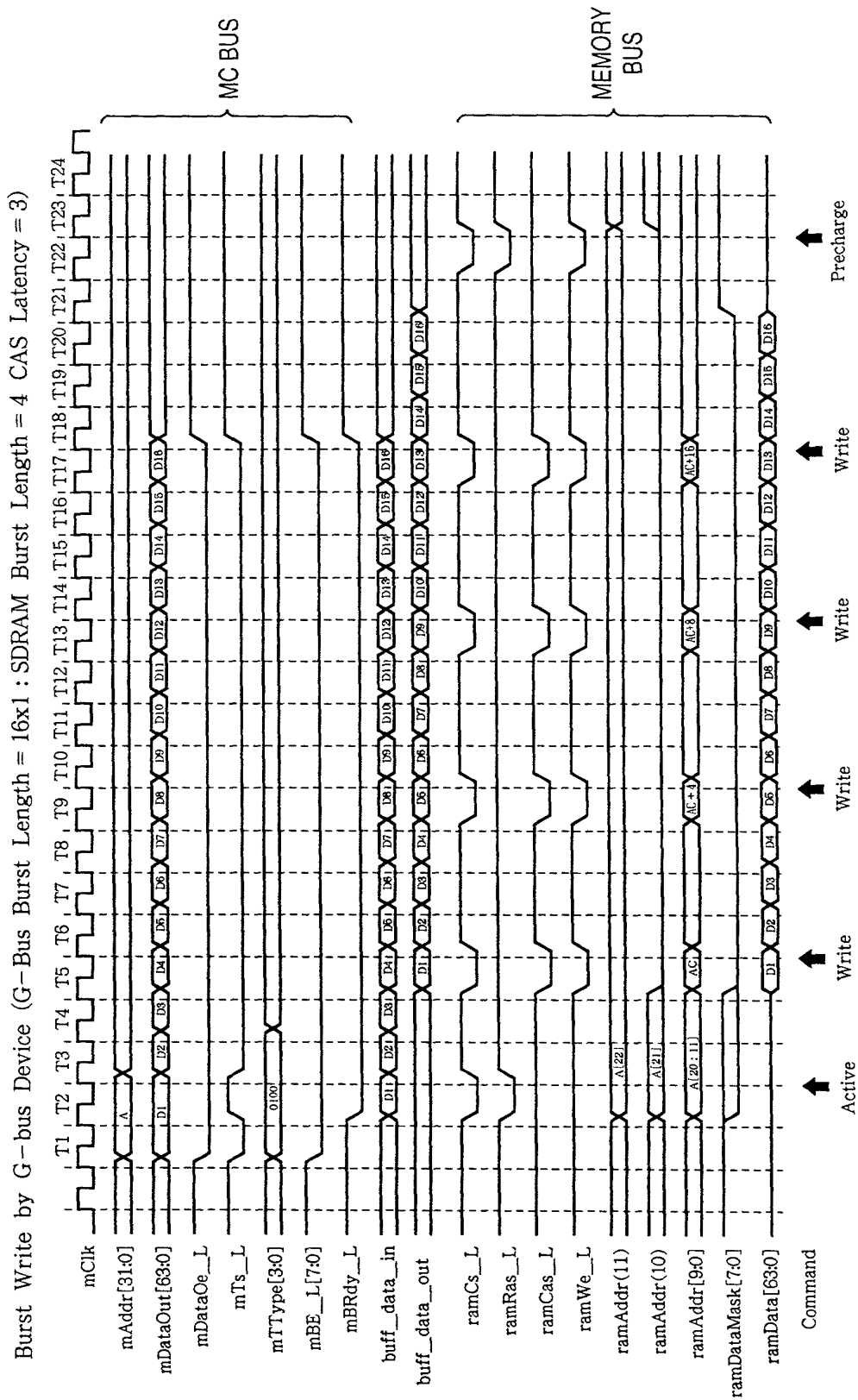


FIG. 15

FIG. 16

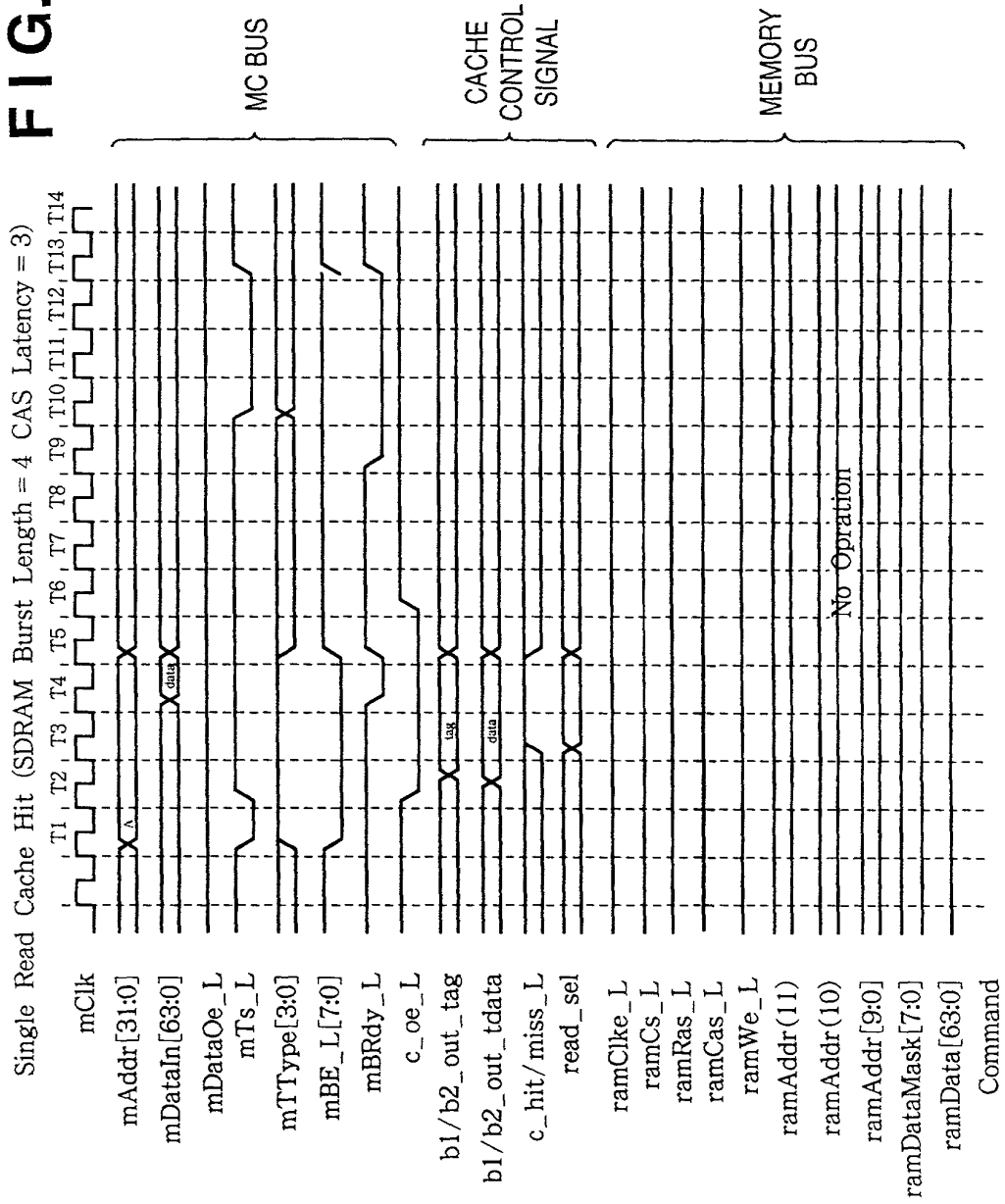




FIG. 17

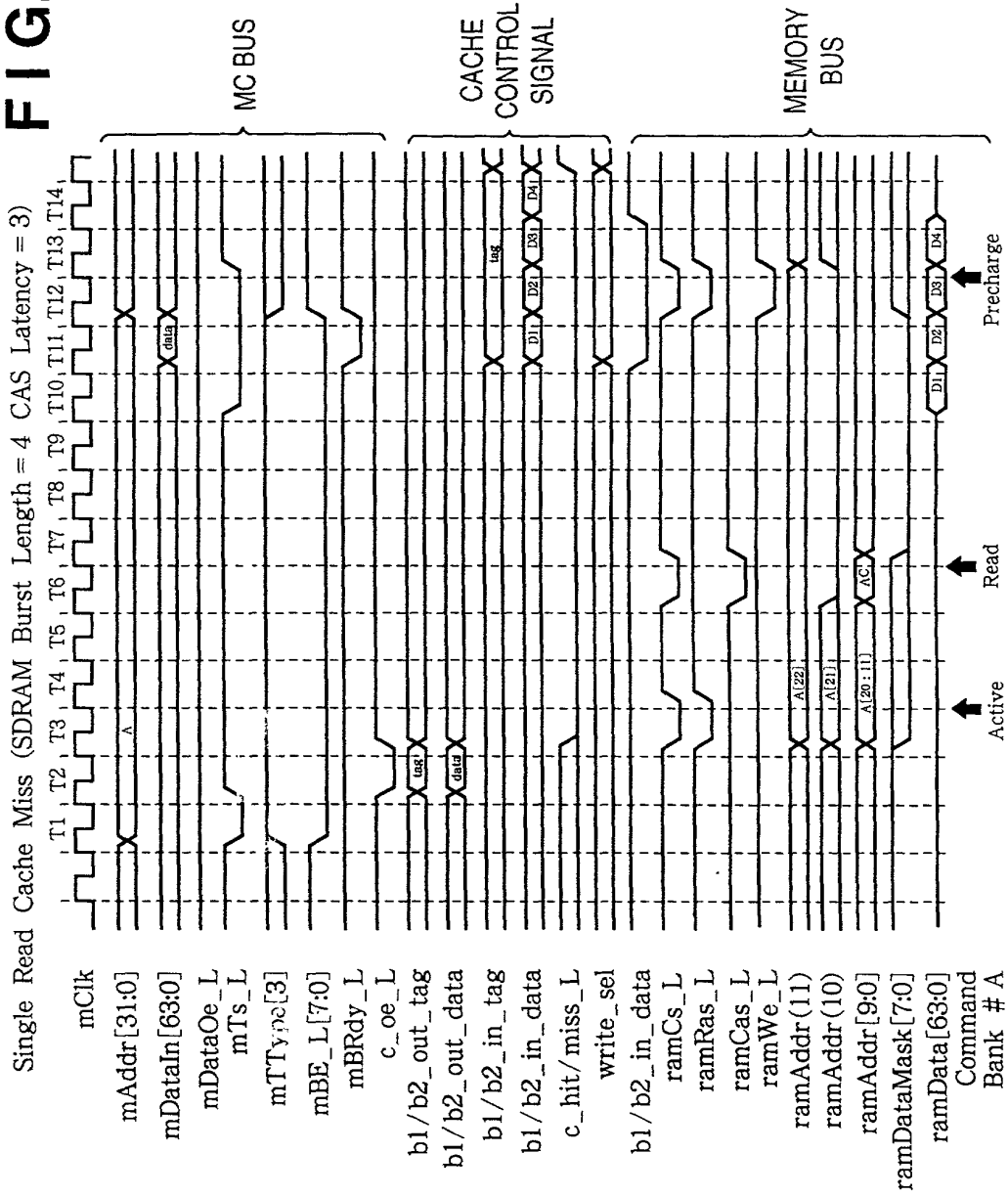
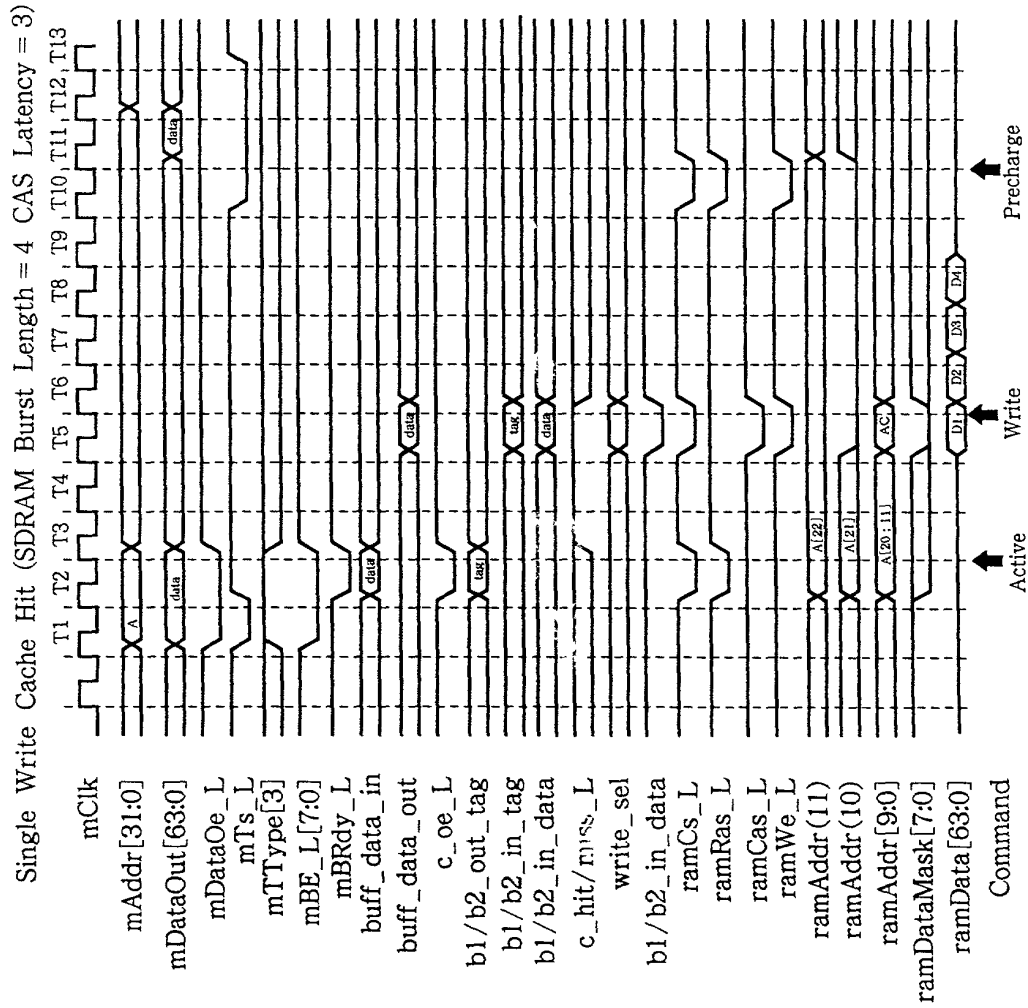


FIG. 18



**FIG. 19**

Single Write Cache Miss (SDRAM Burst Length = 4 CAS Latency = 3)

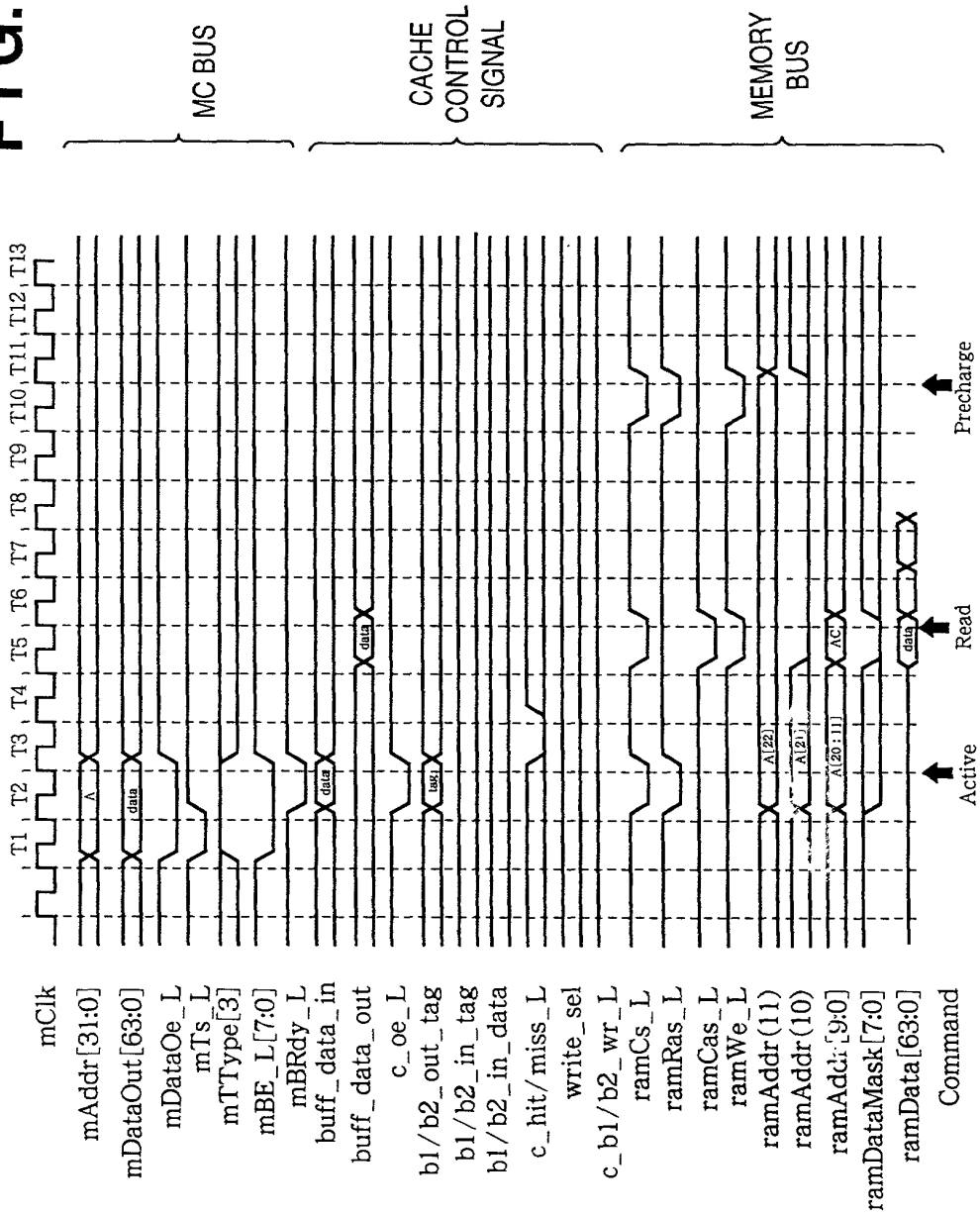
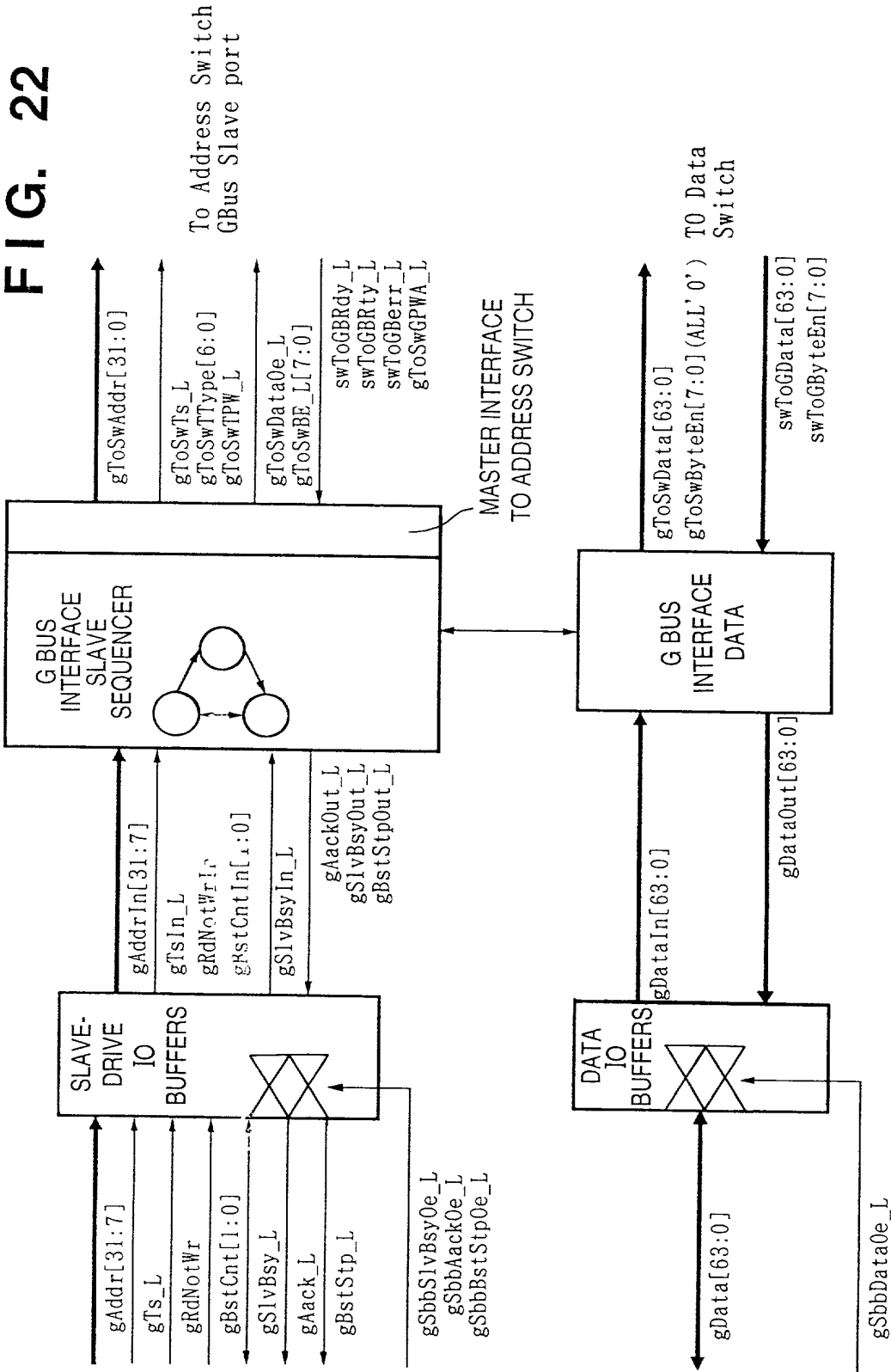






FIG. 22



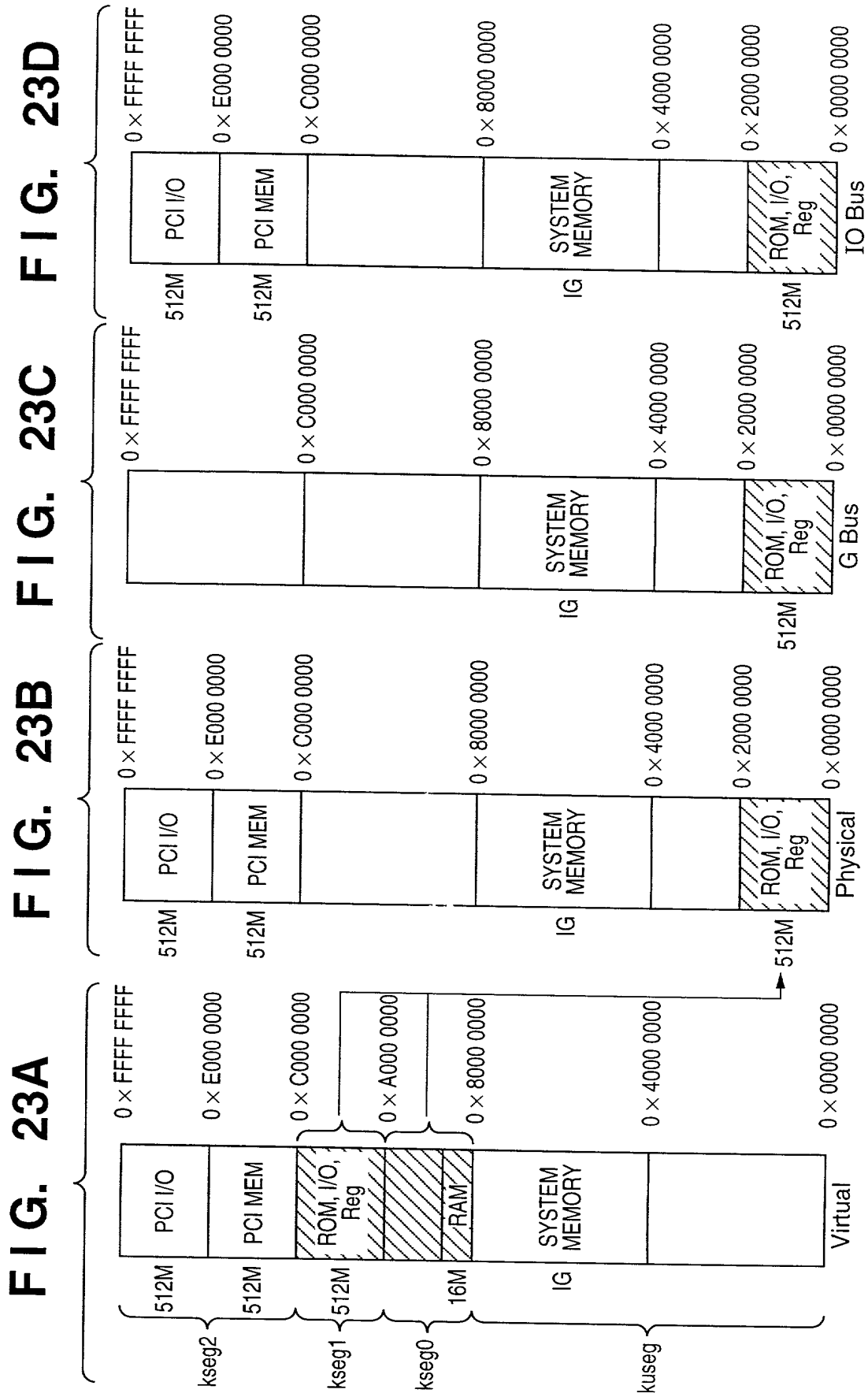


FIG. 24A

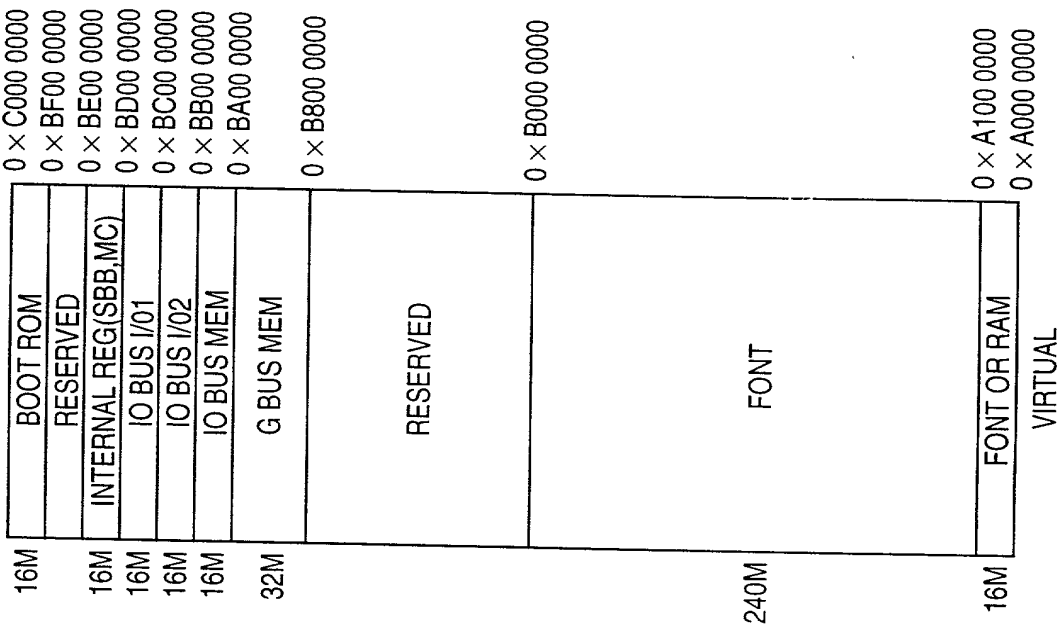


FIG. 24B

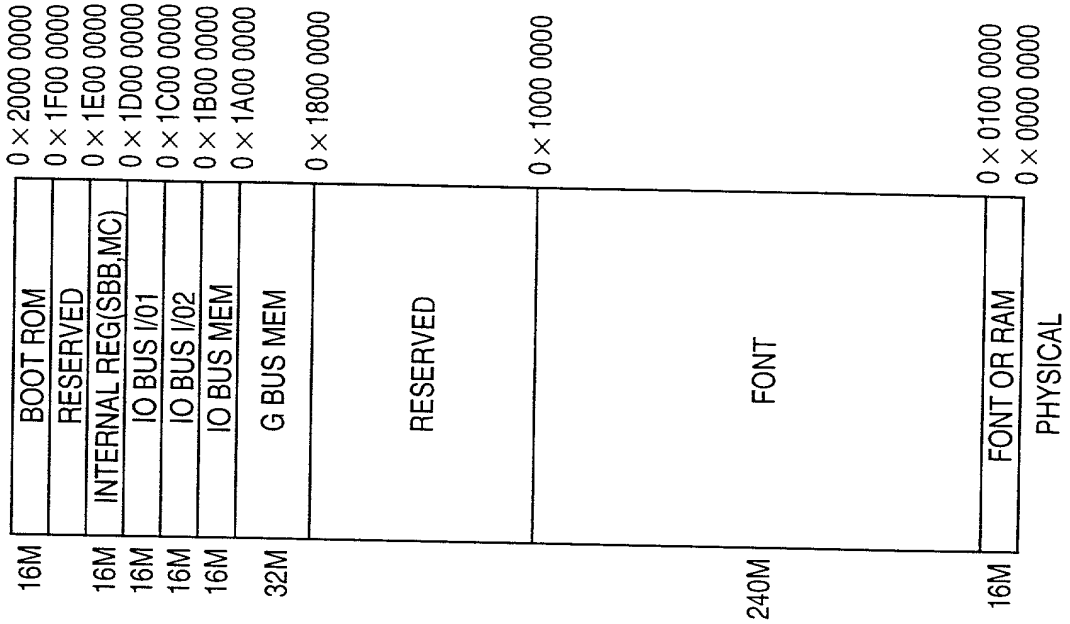




FIG. 24C

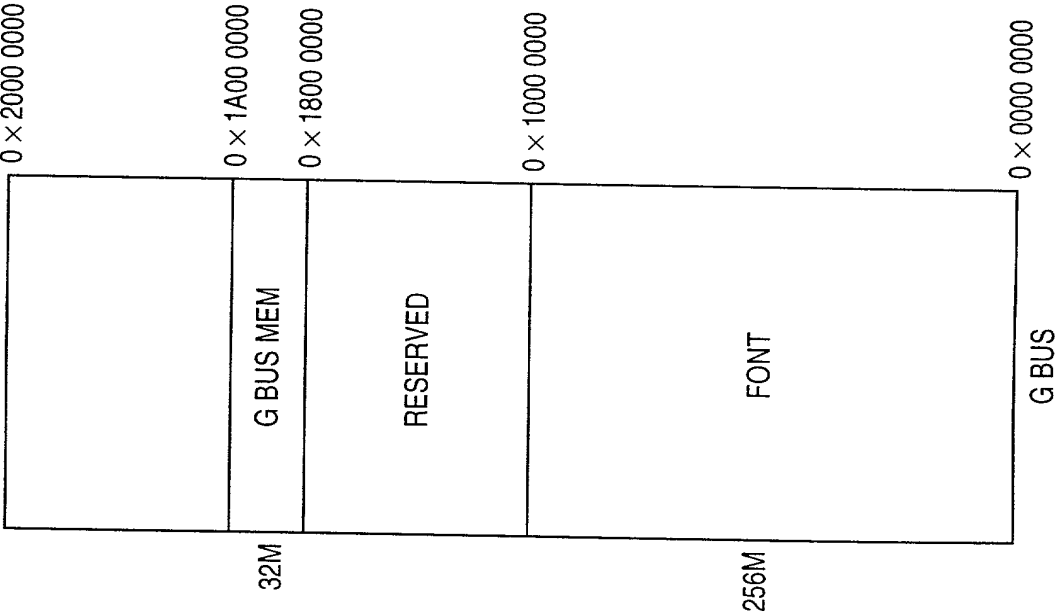
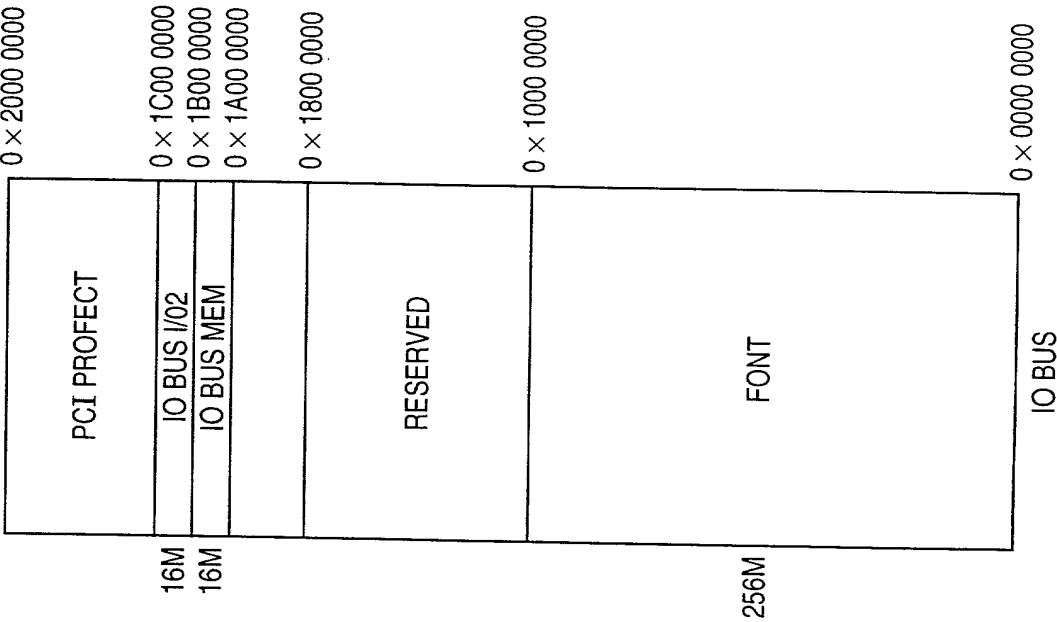


FIG. 24D



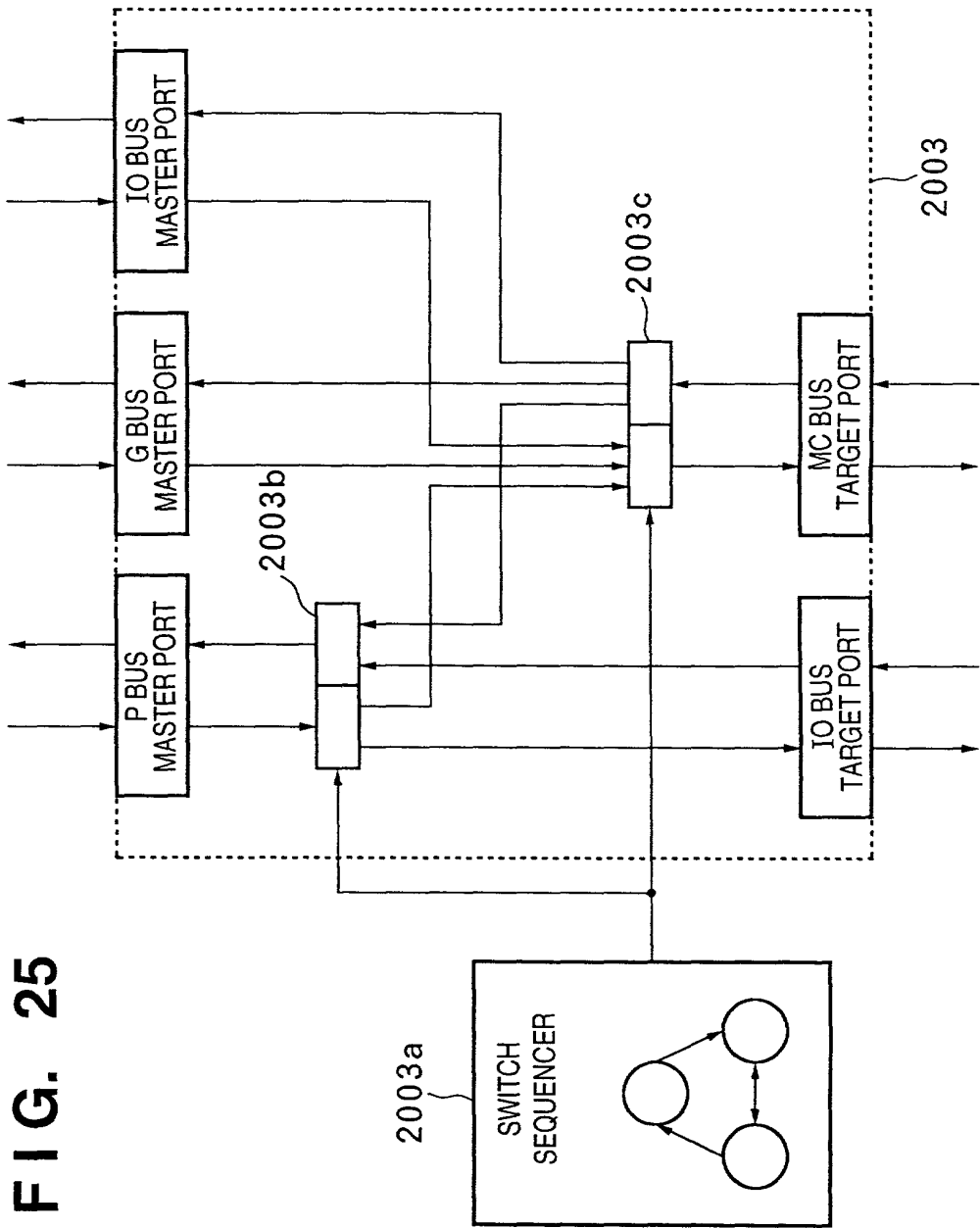
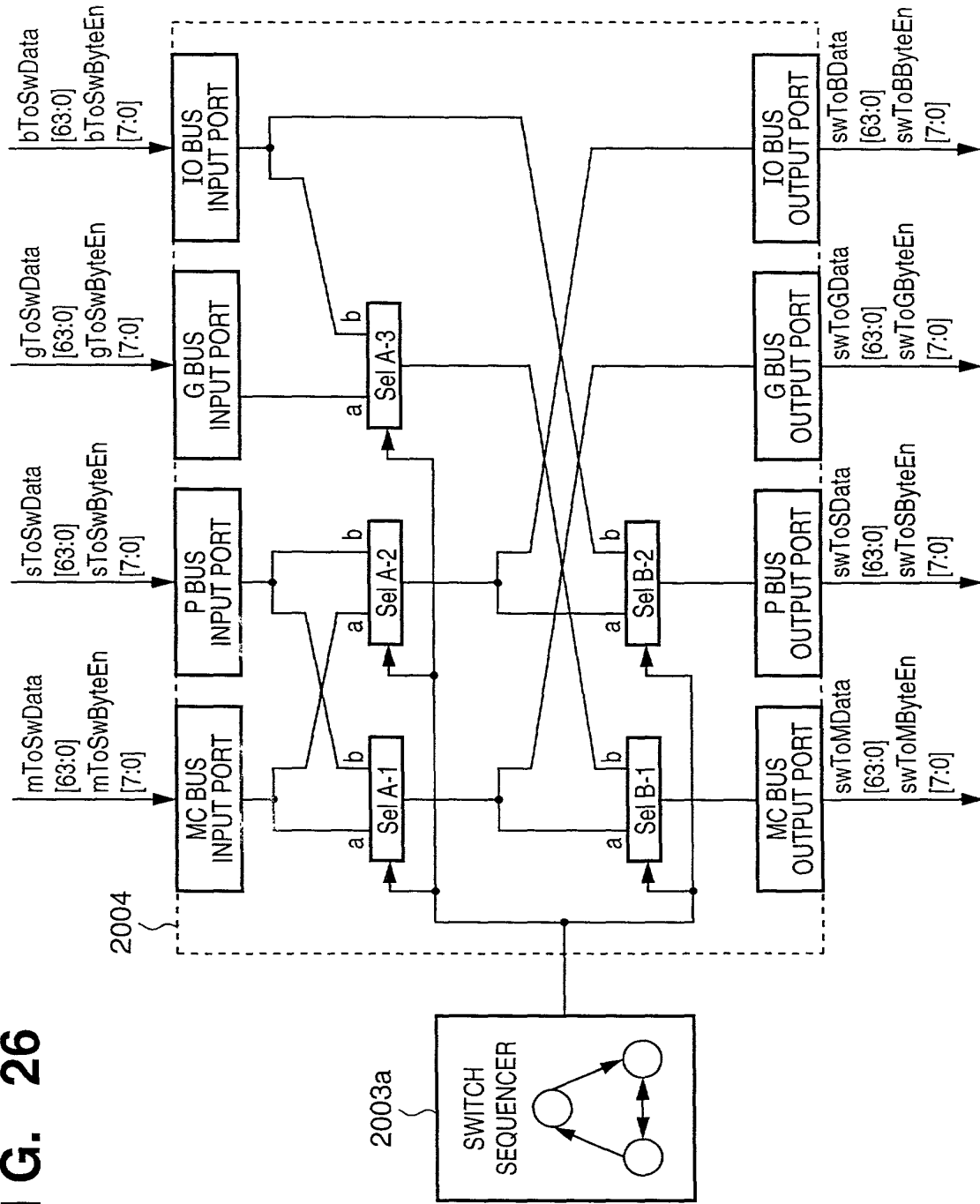


FIG. 26



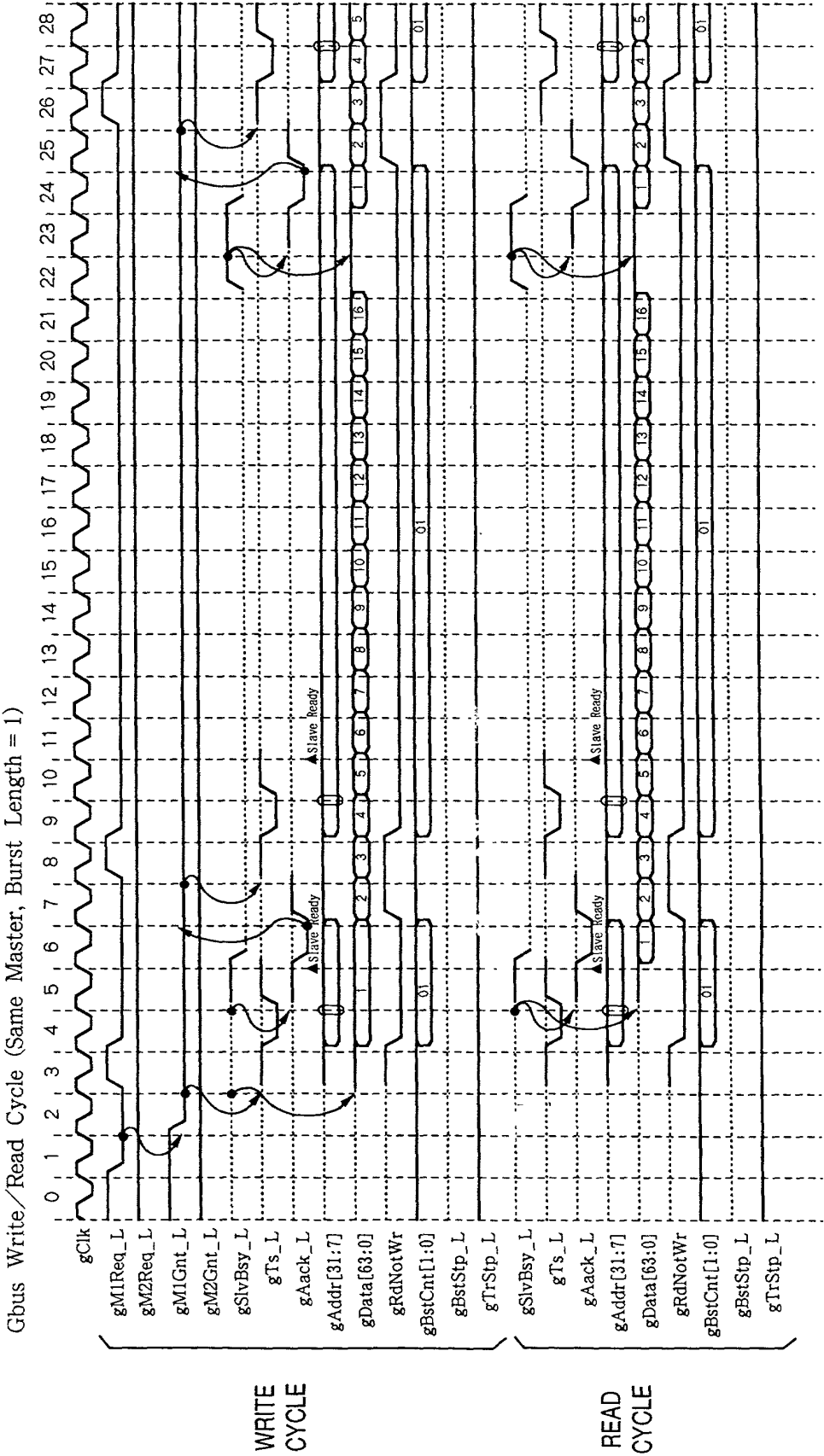


FIG. 27

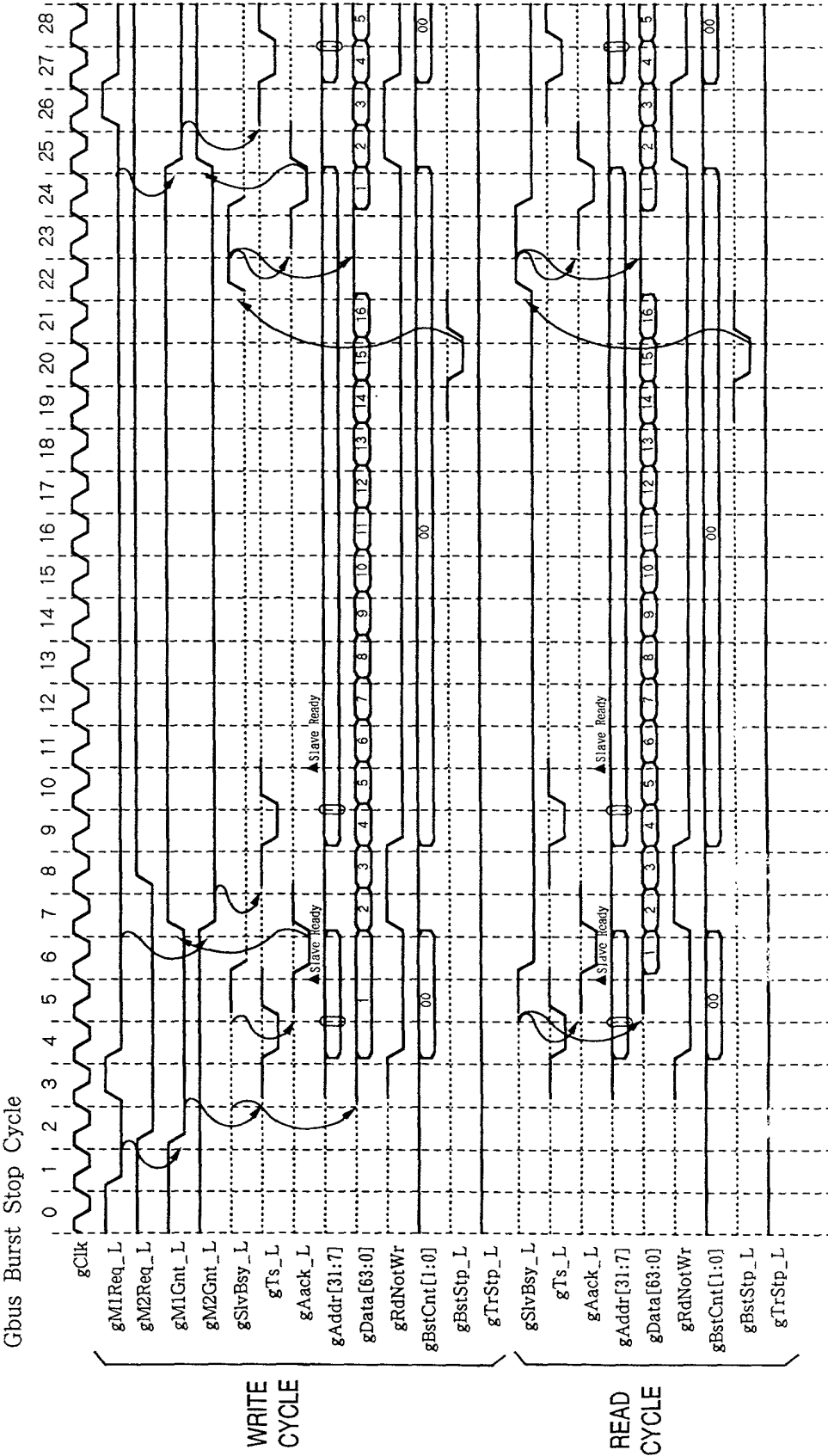
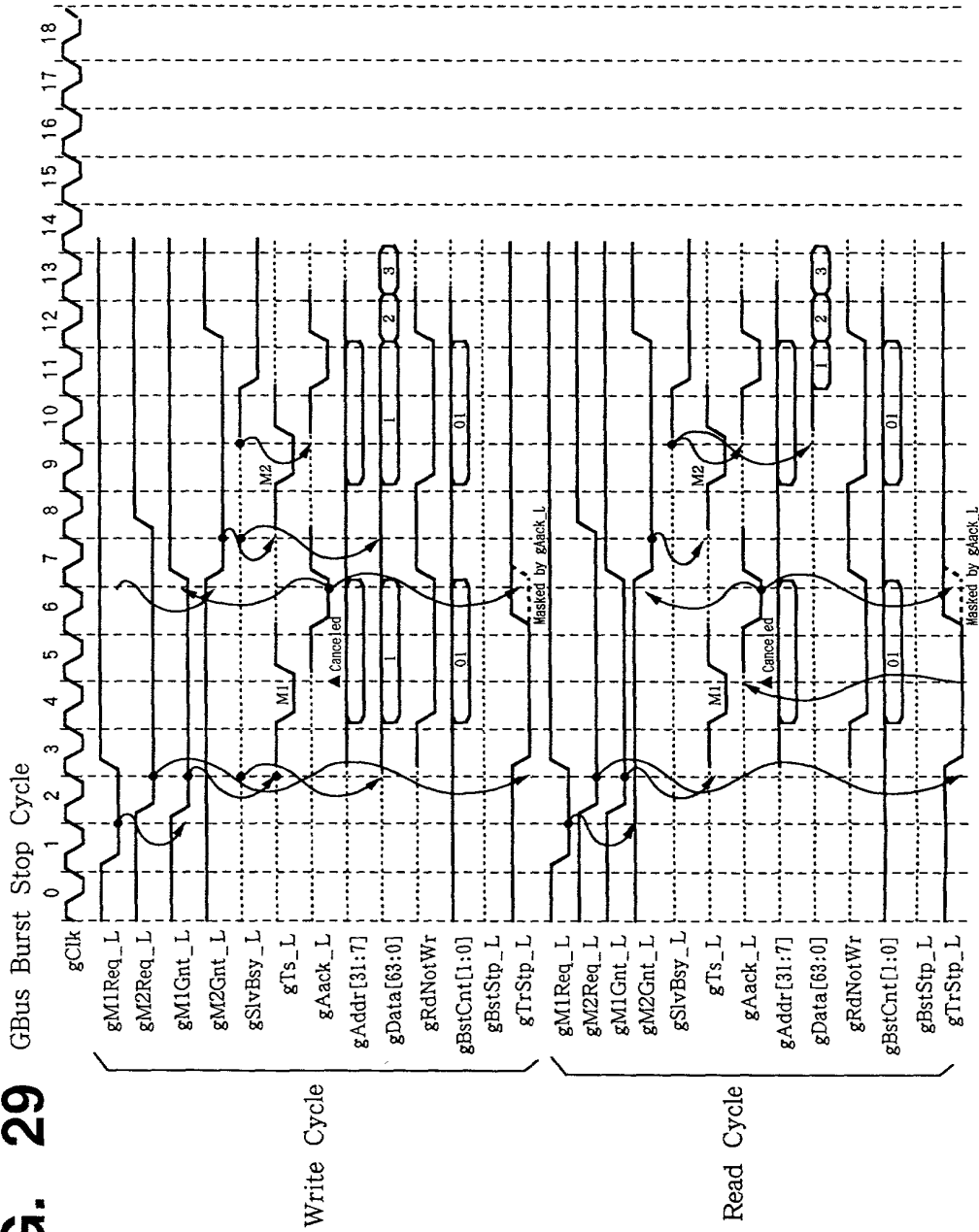
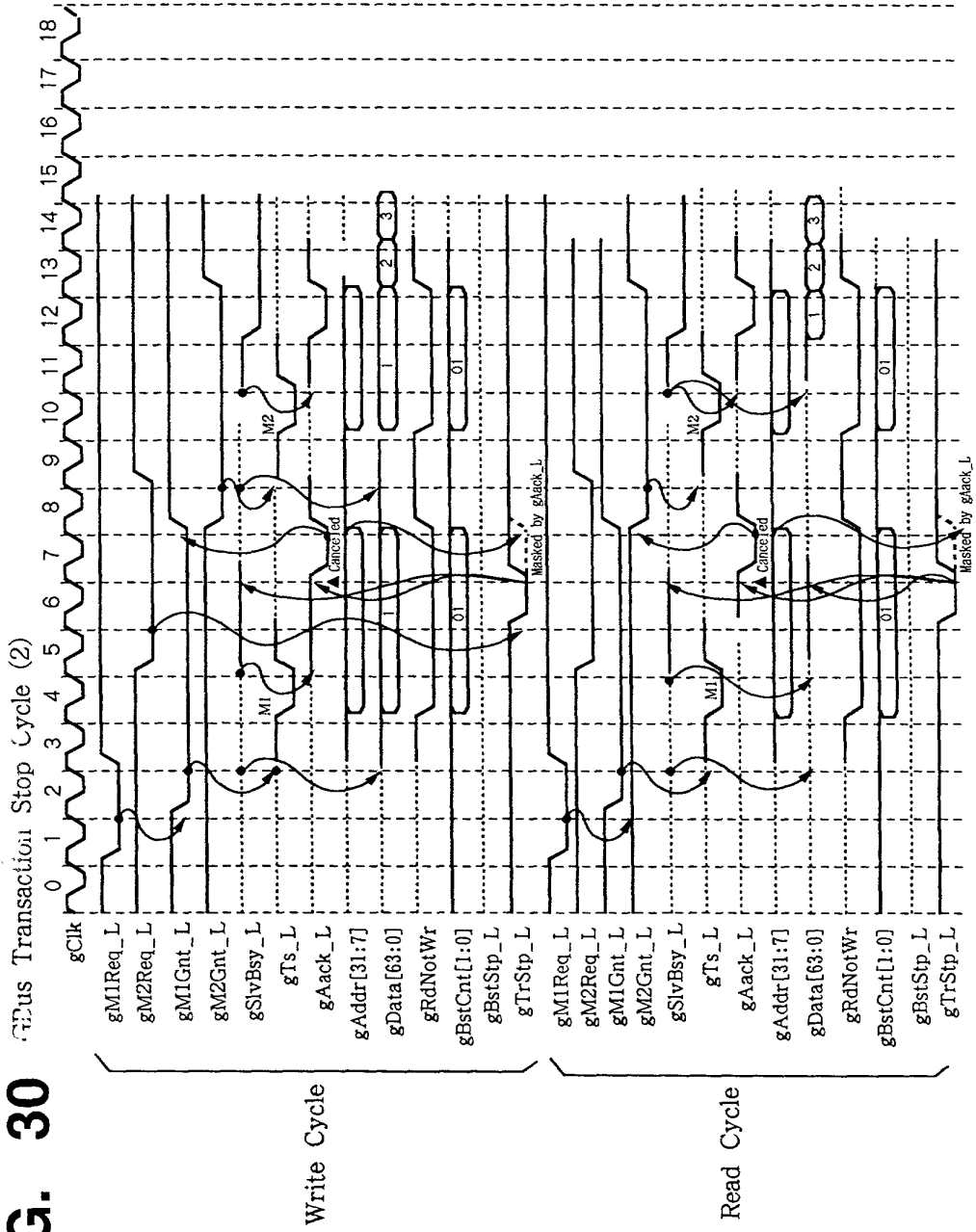


FIG. 28

FIG. 29



**FIG. 30**



**FIG. 31**

GBus Transaction Stop Cycle (3)

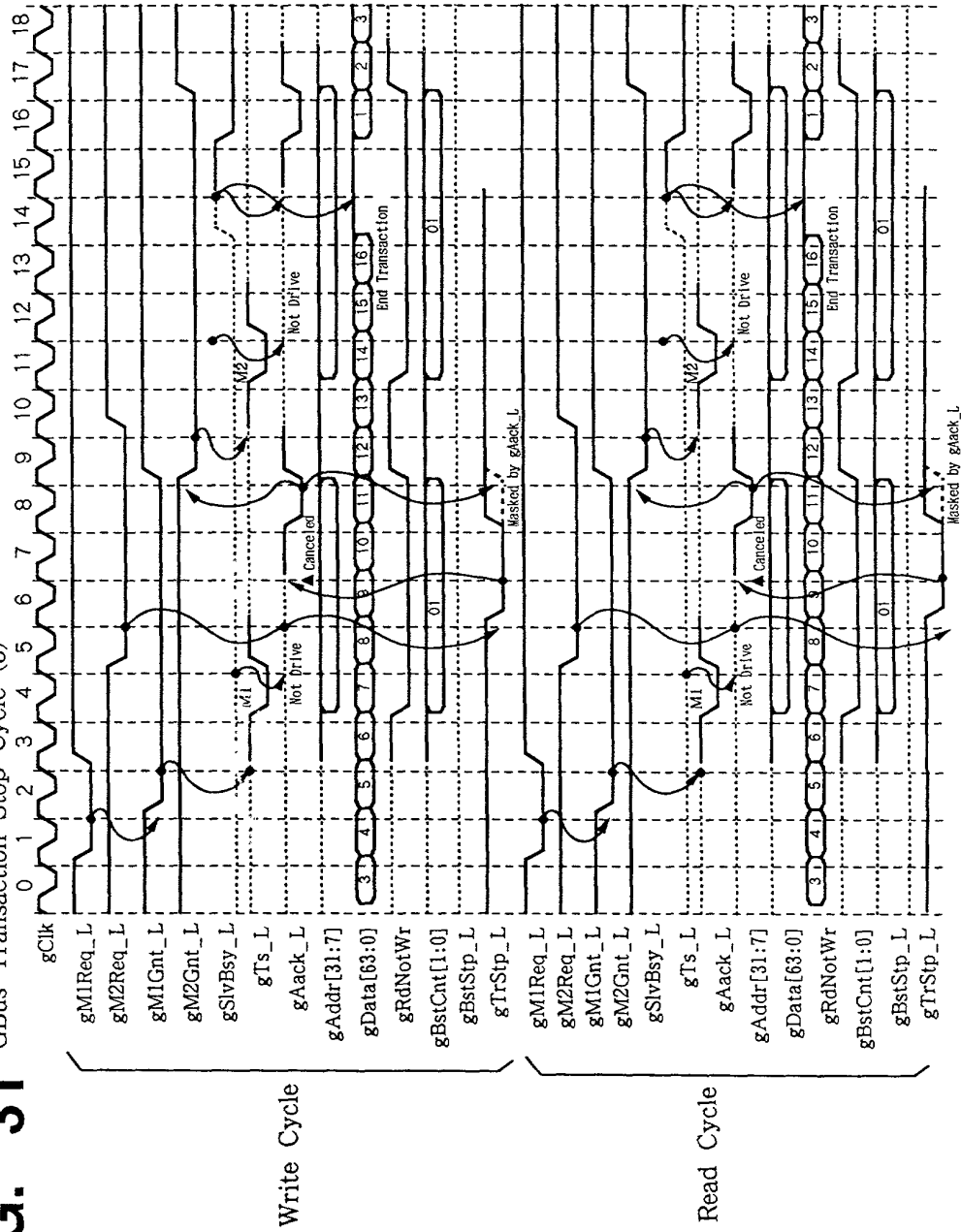
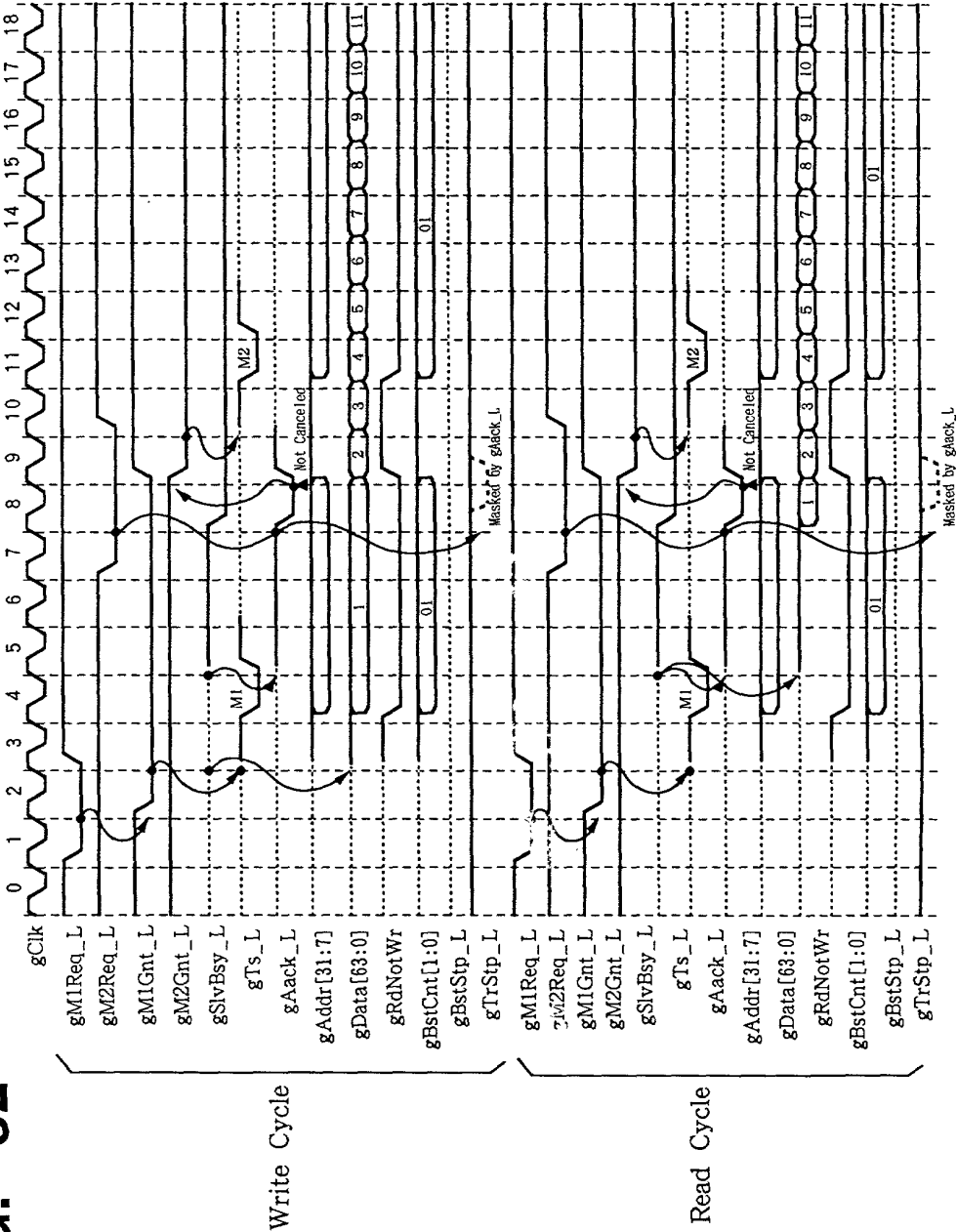




FIG. 32

GBus Transaction Stop Cycle (4)



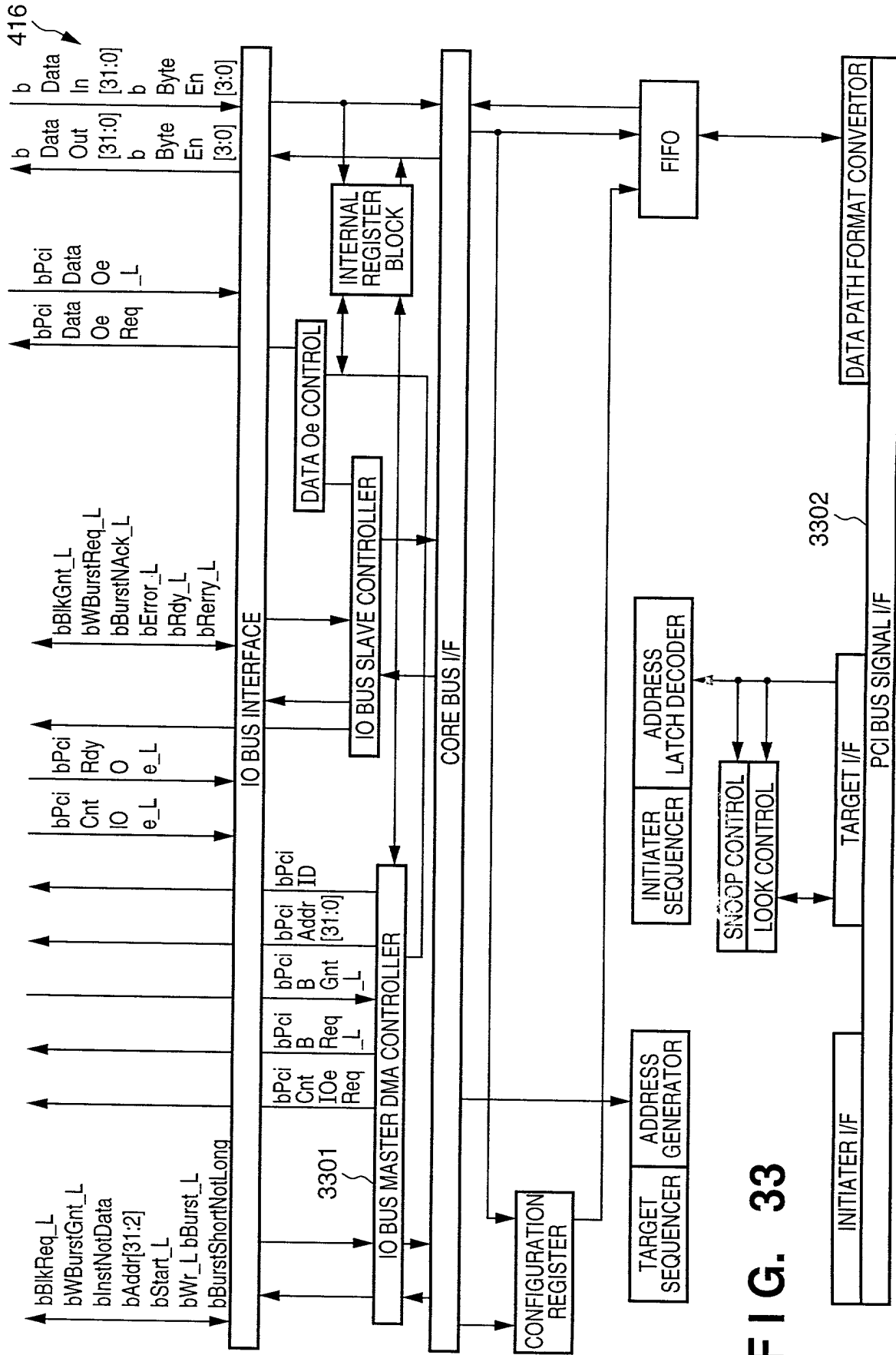
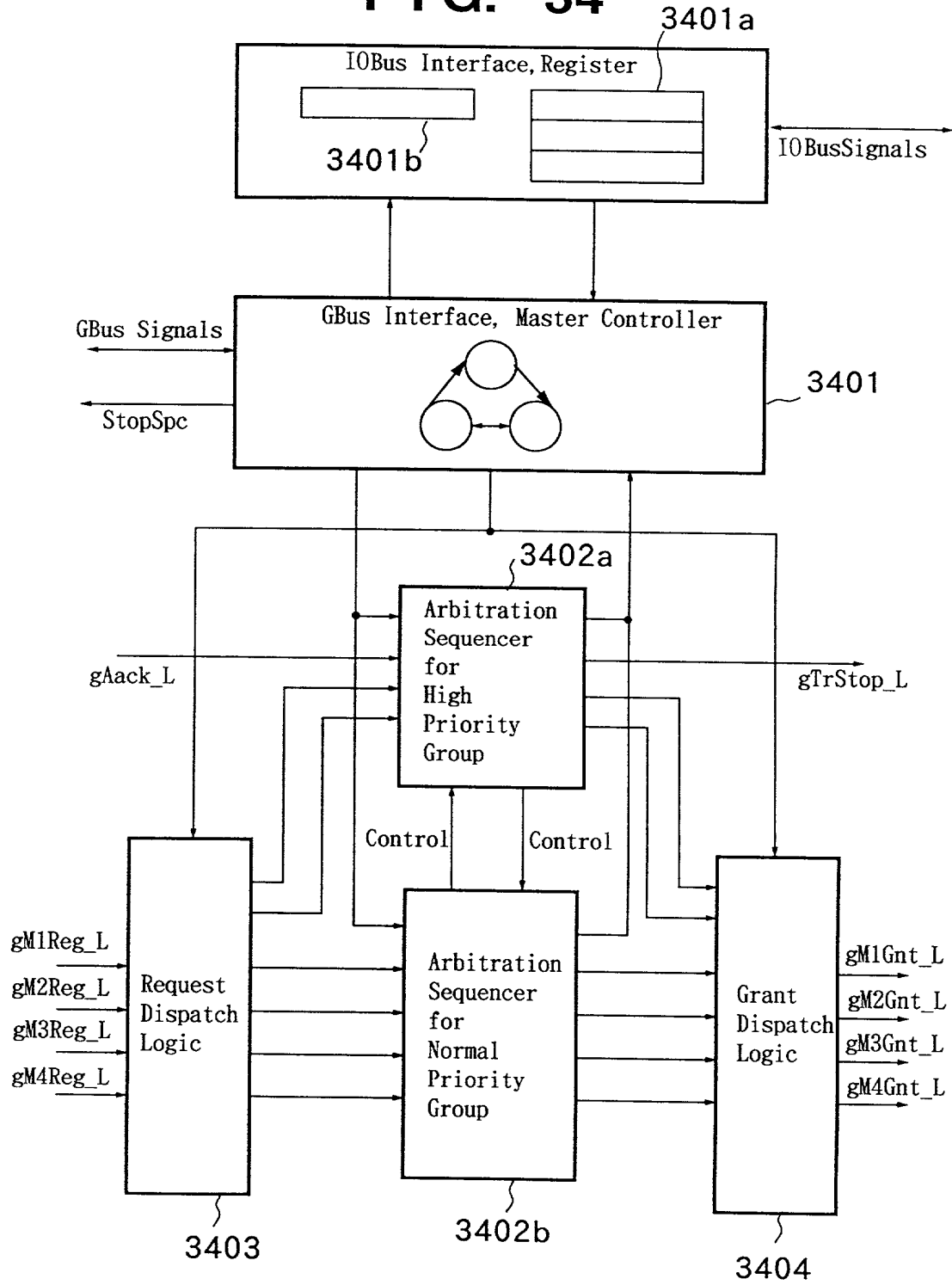


FIG. 33

**FIG. 34**

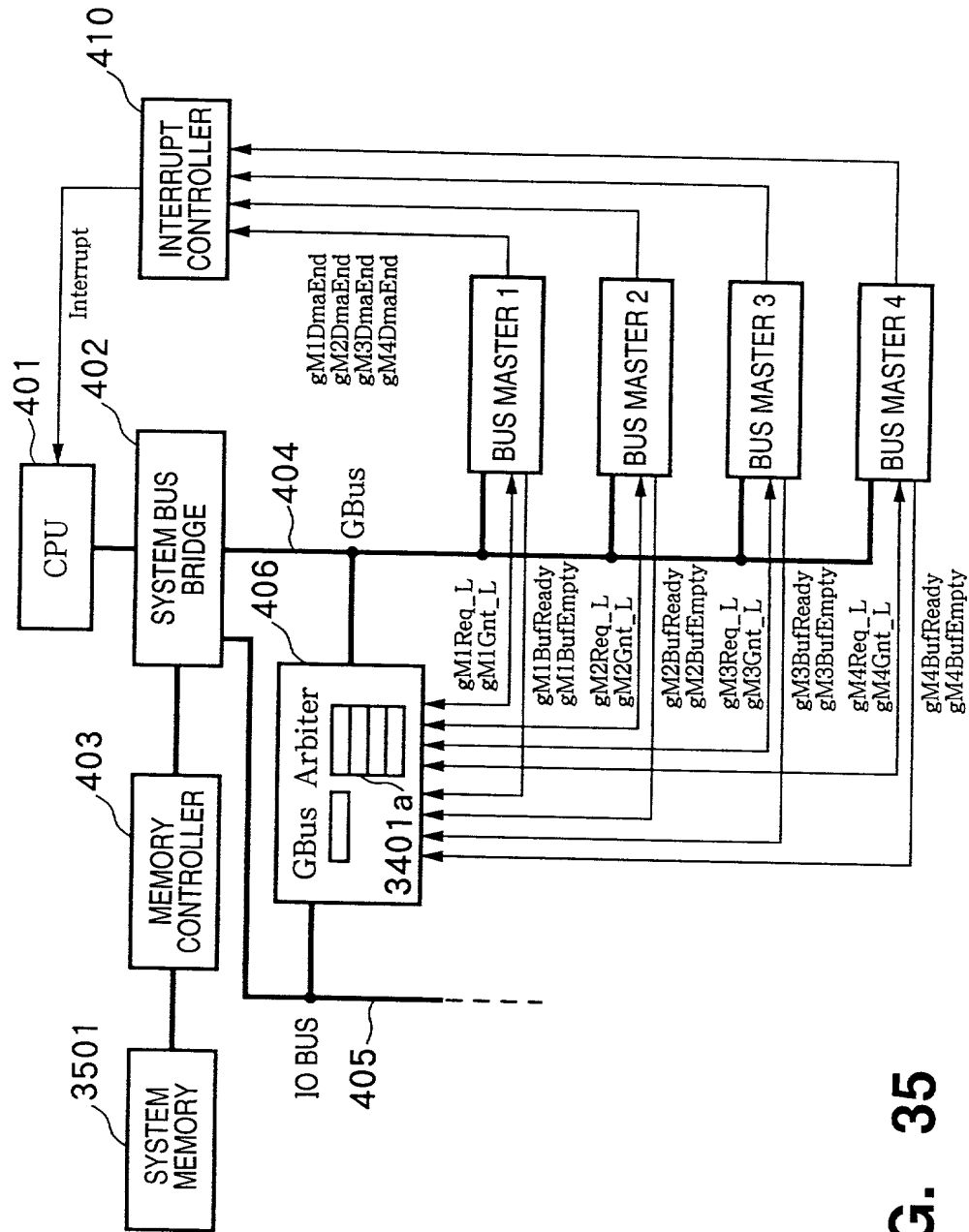


FIG. 35

FIG. 36

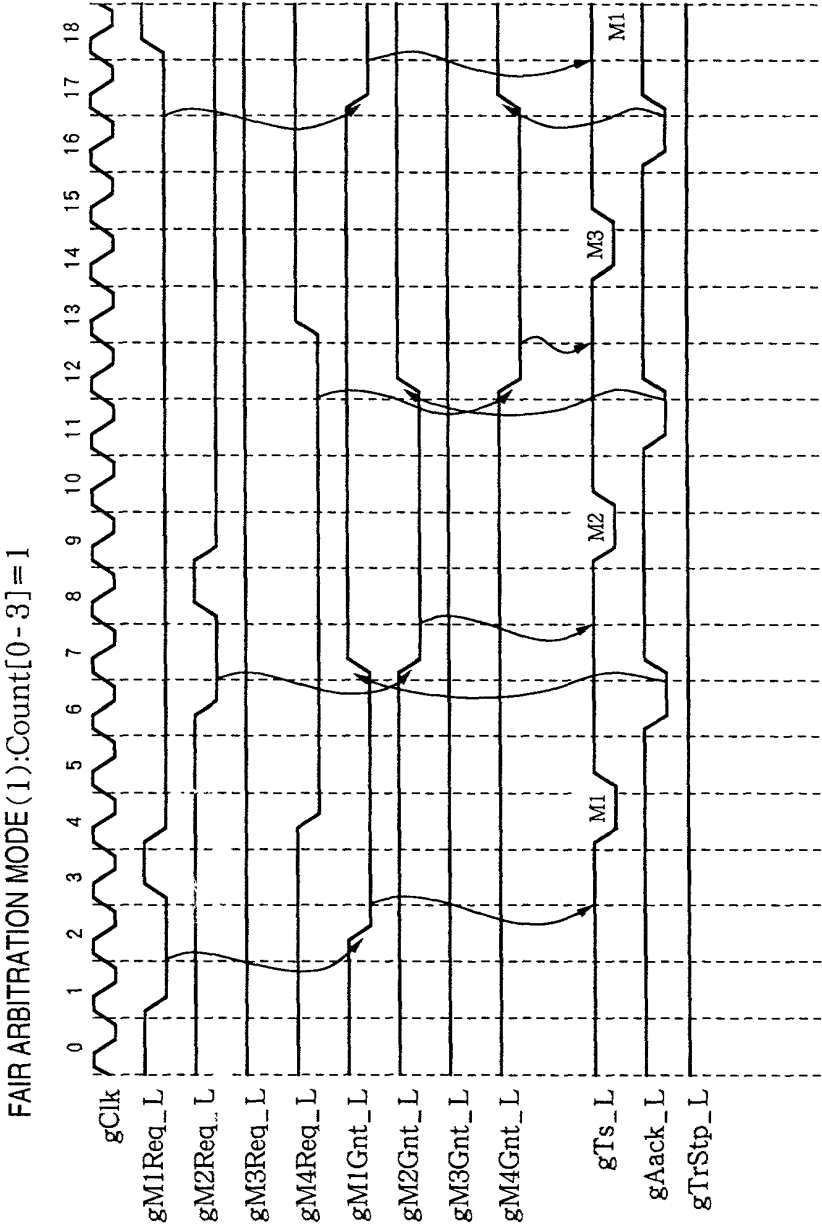


FIG. 37

FAIR ARBITRATION MODE (2):Count[0]=2,Count[1-3]=1

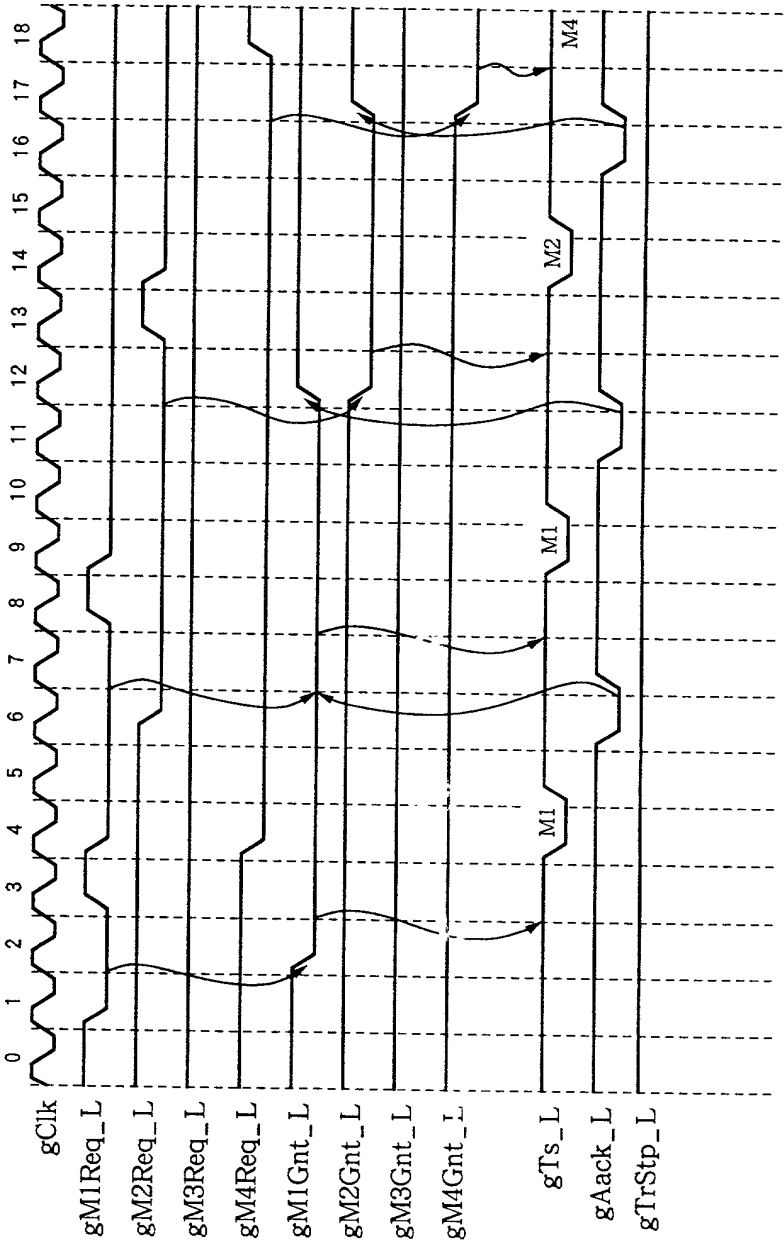
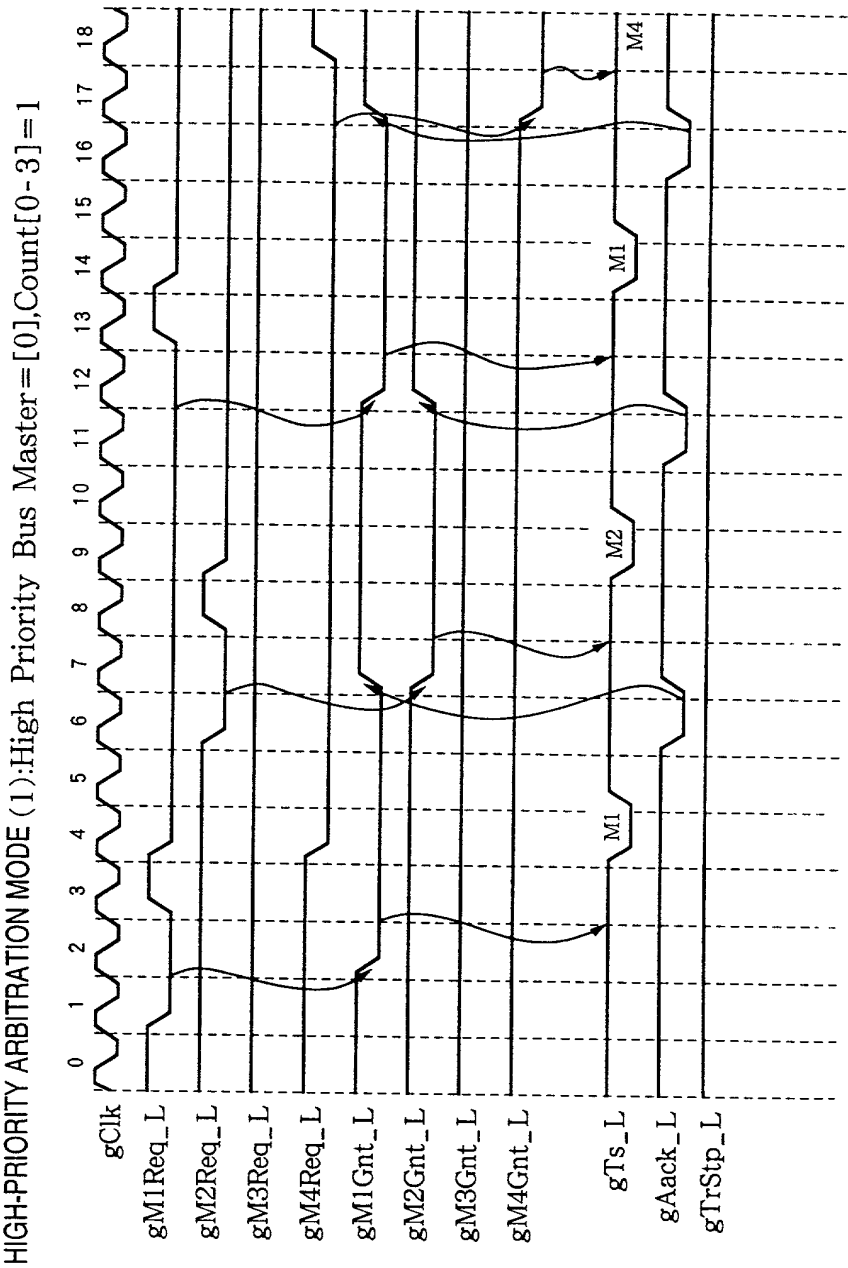


FIG. 38



**FIG. 39**

TRANSACTION STOP CYCLE (1): High Priority Bus Master = [0]

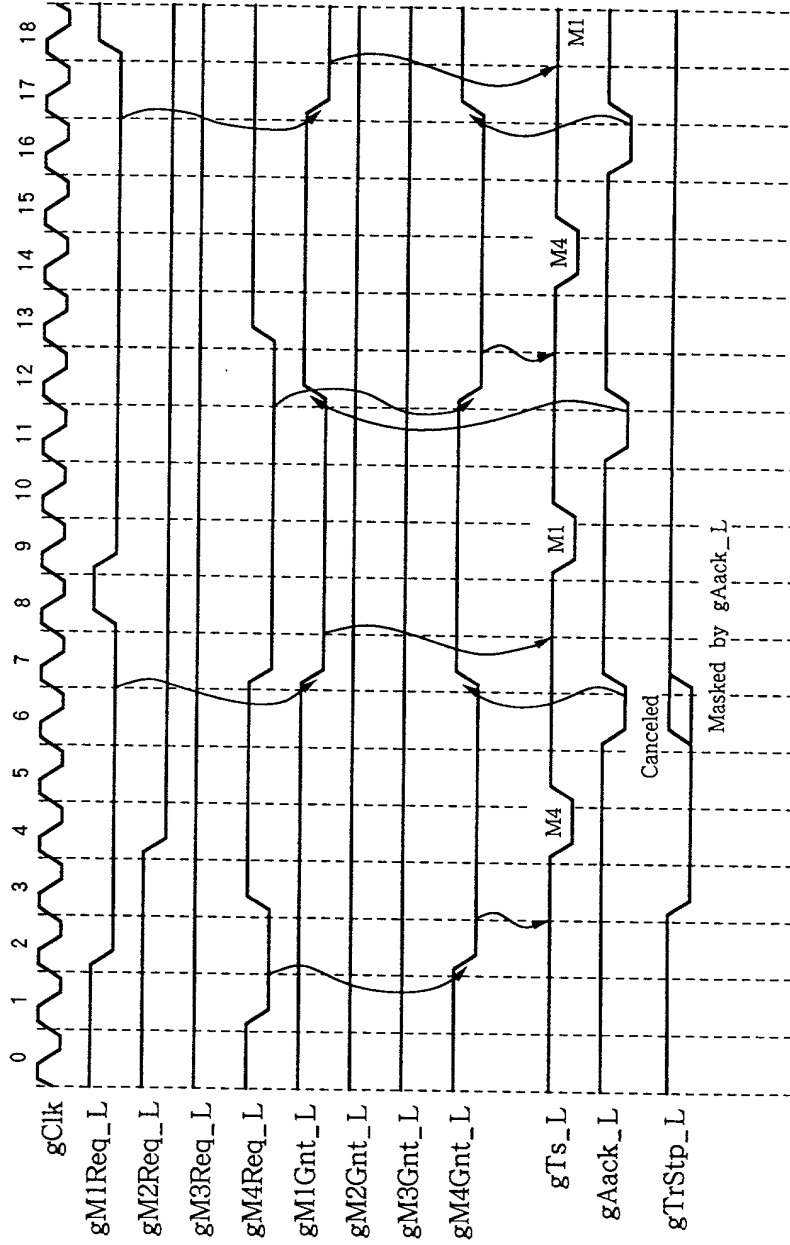
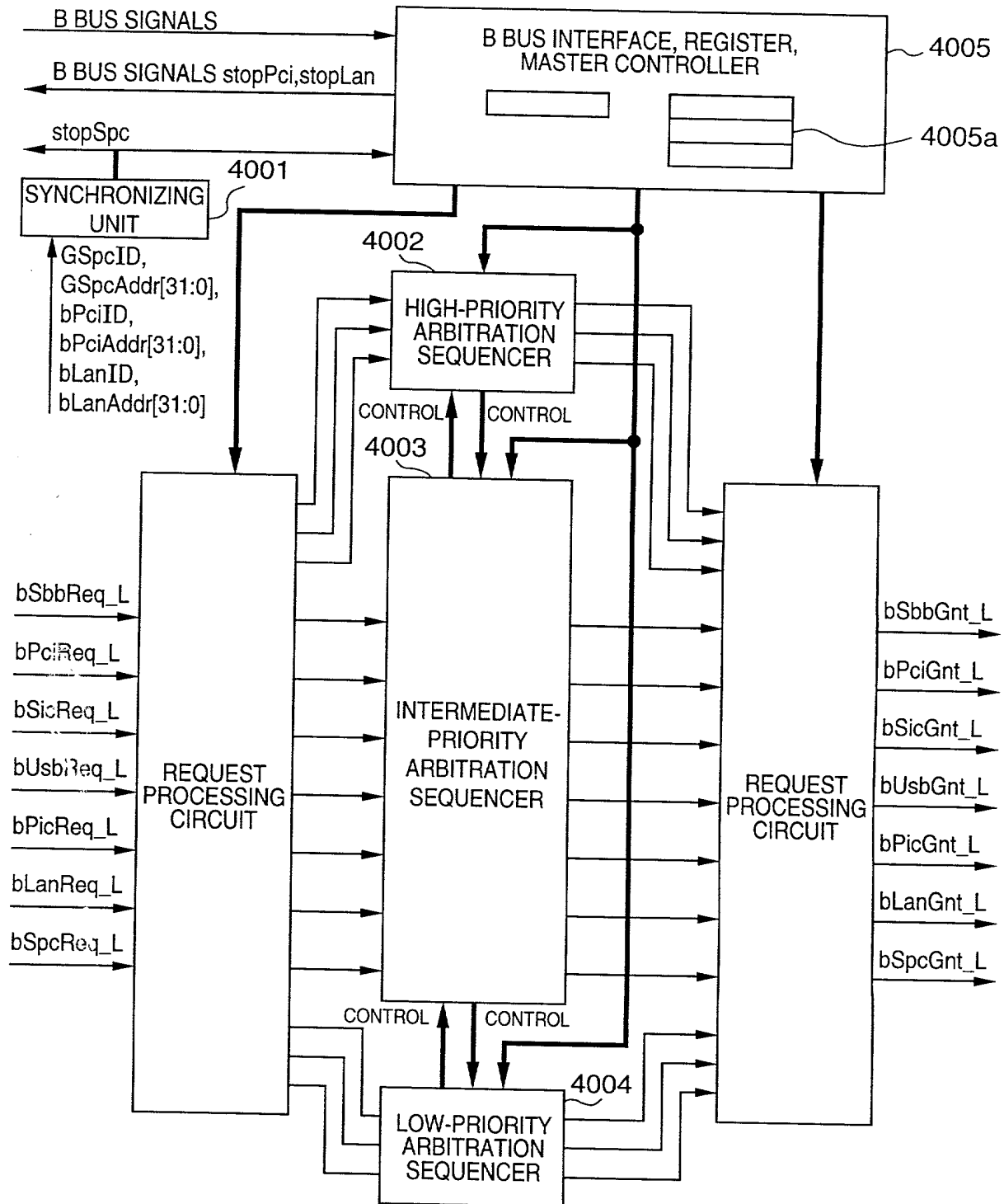




FIG. 40



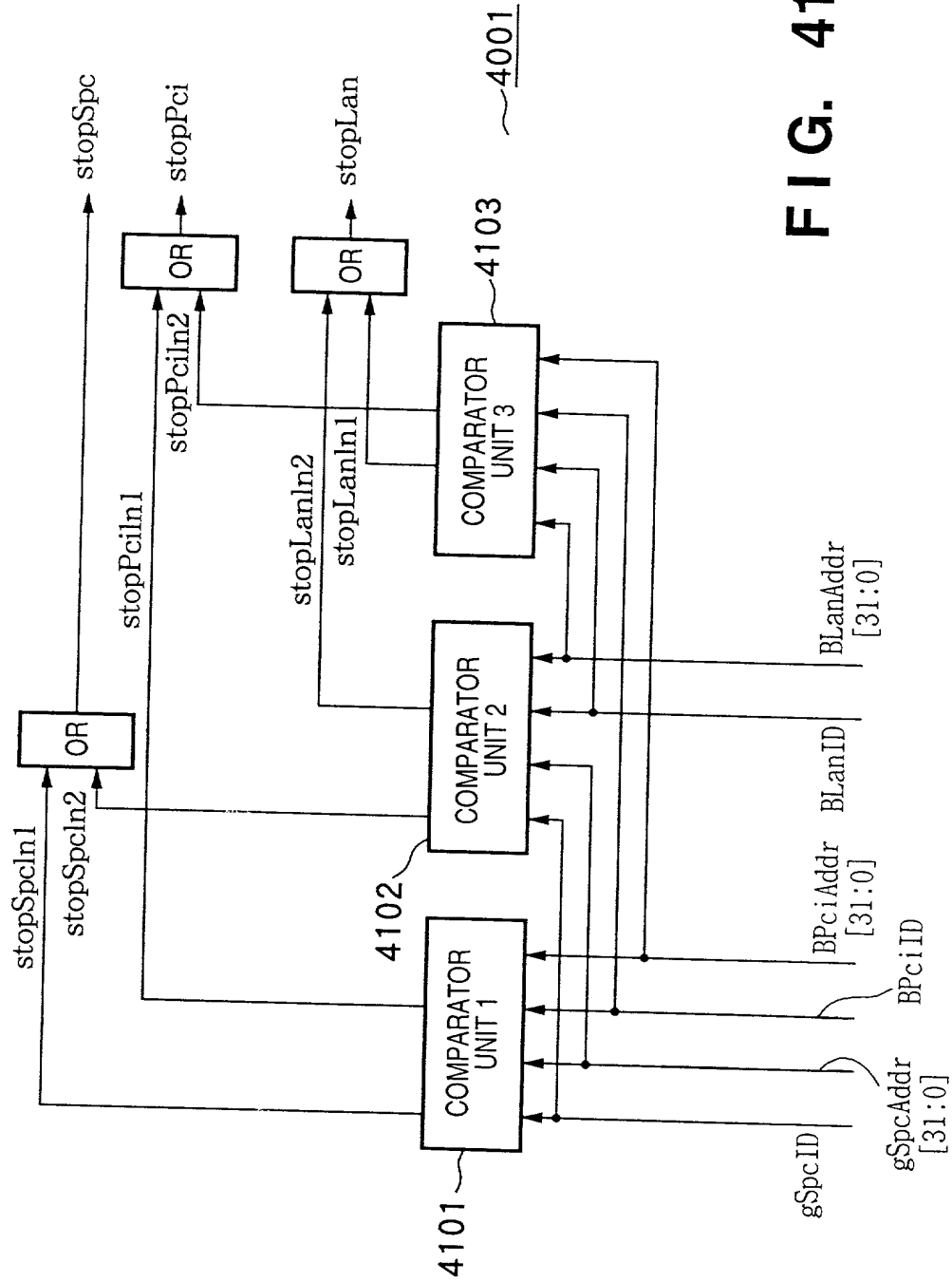


FIG. 41

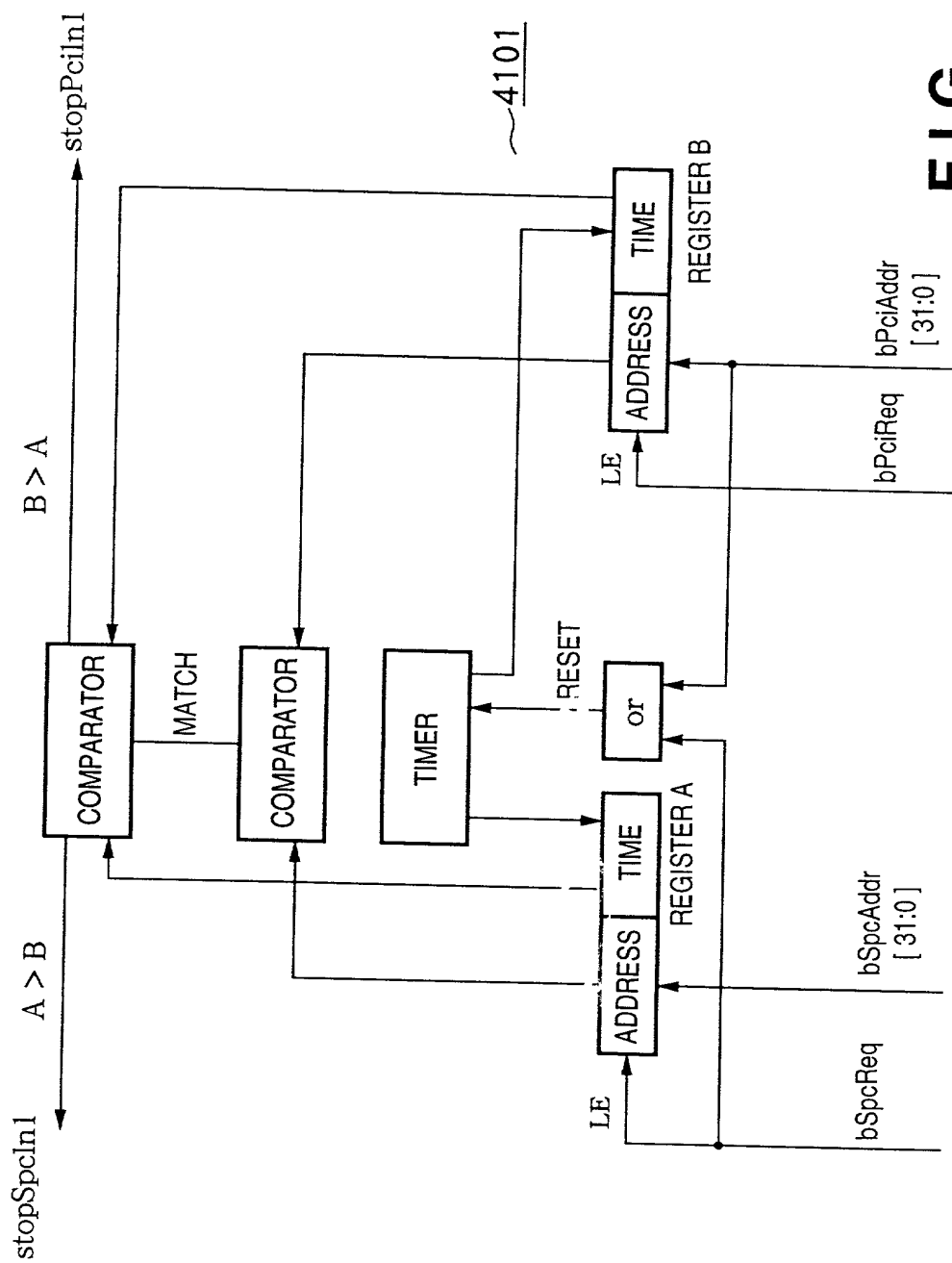
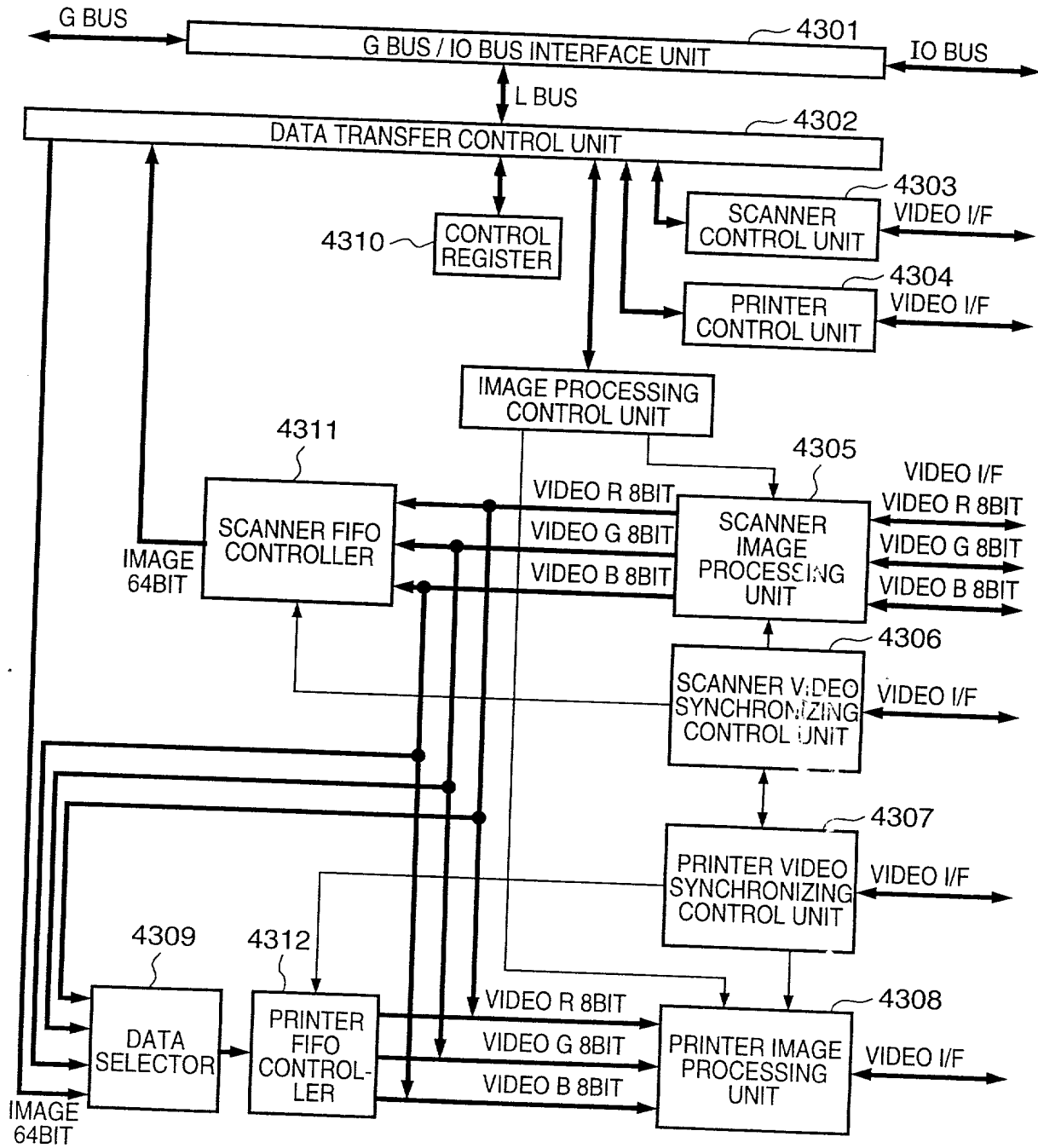
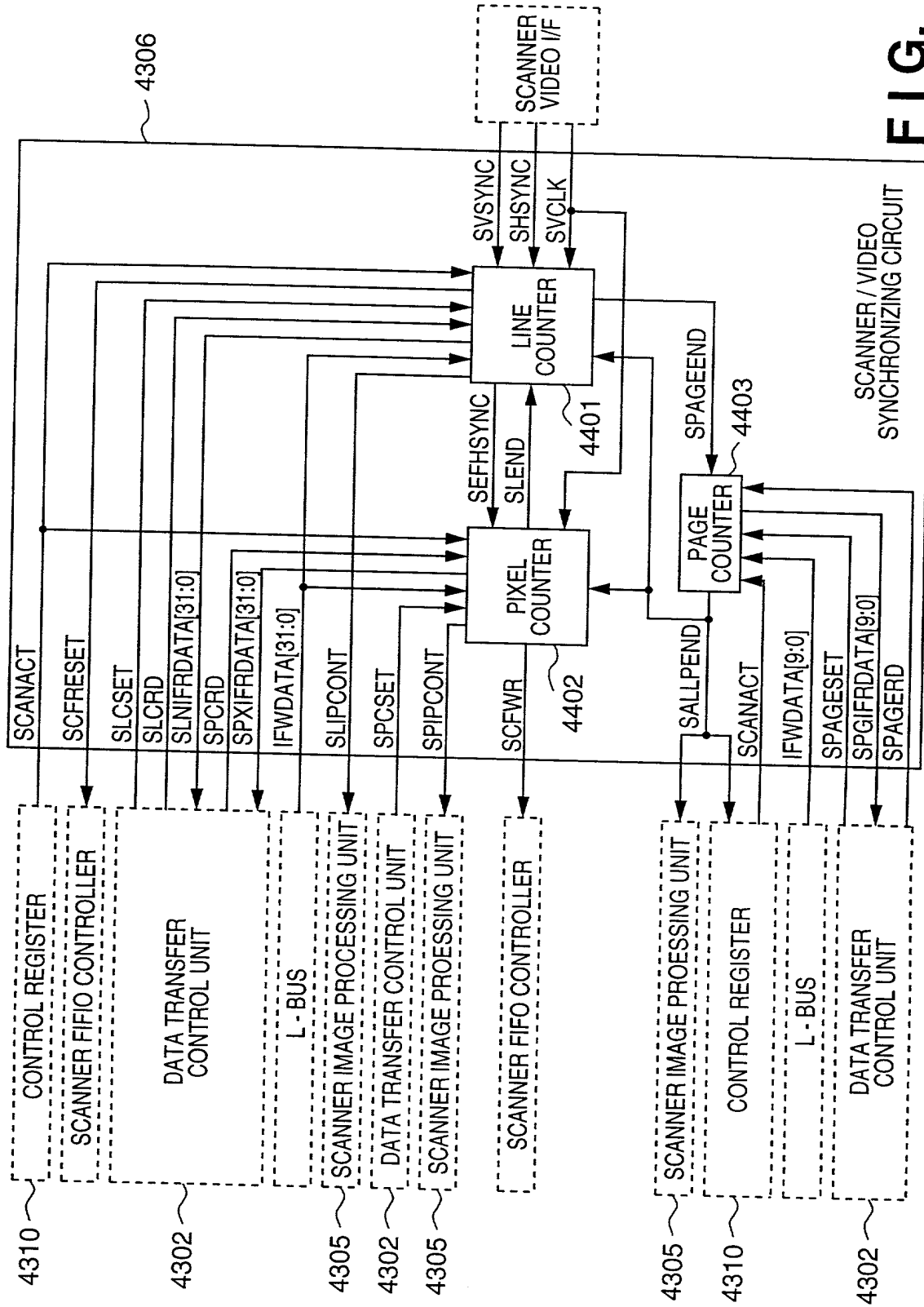


FIG. 42

FIG. 43





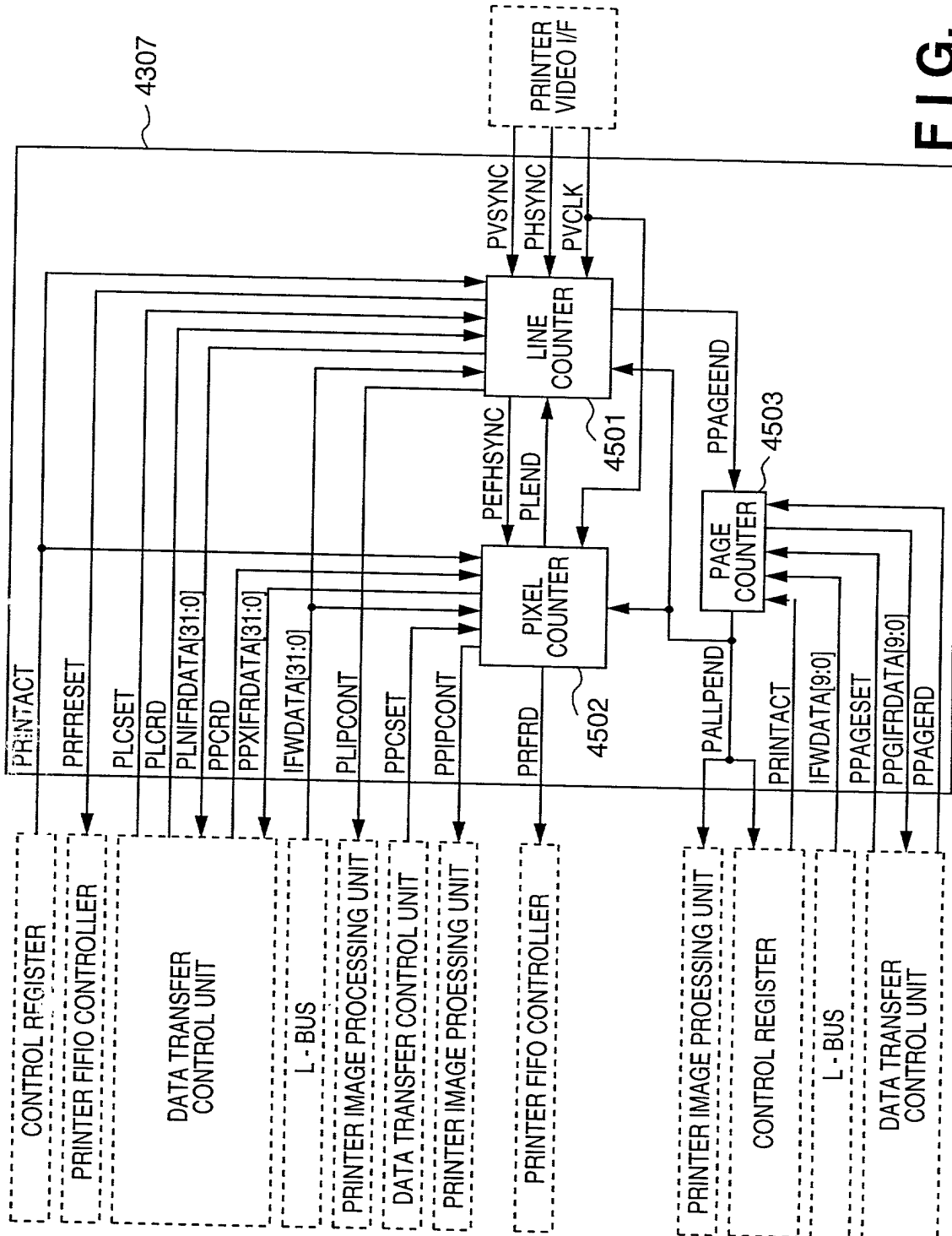
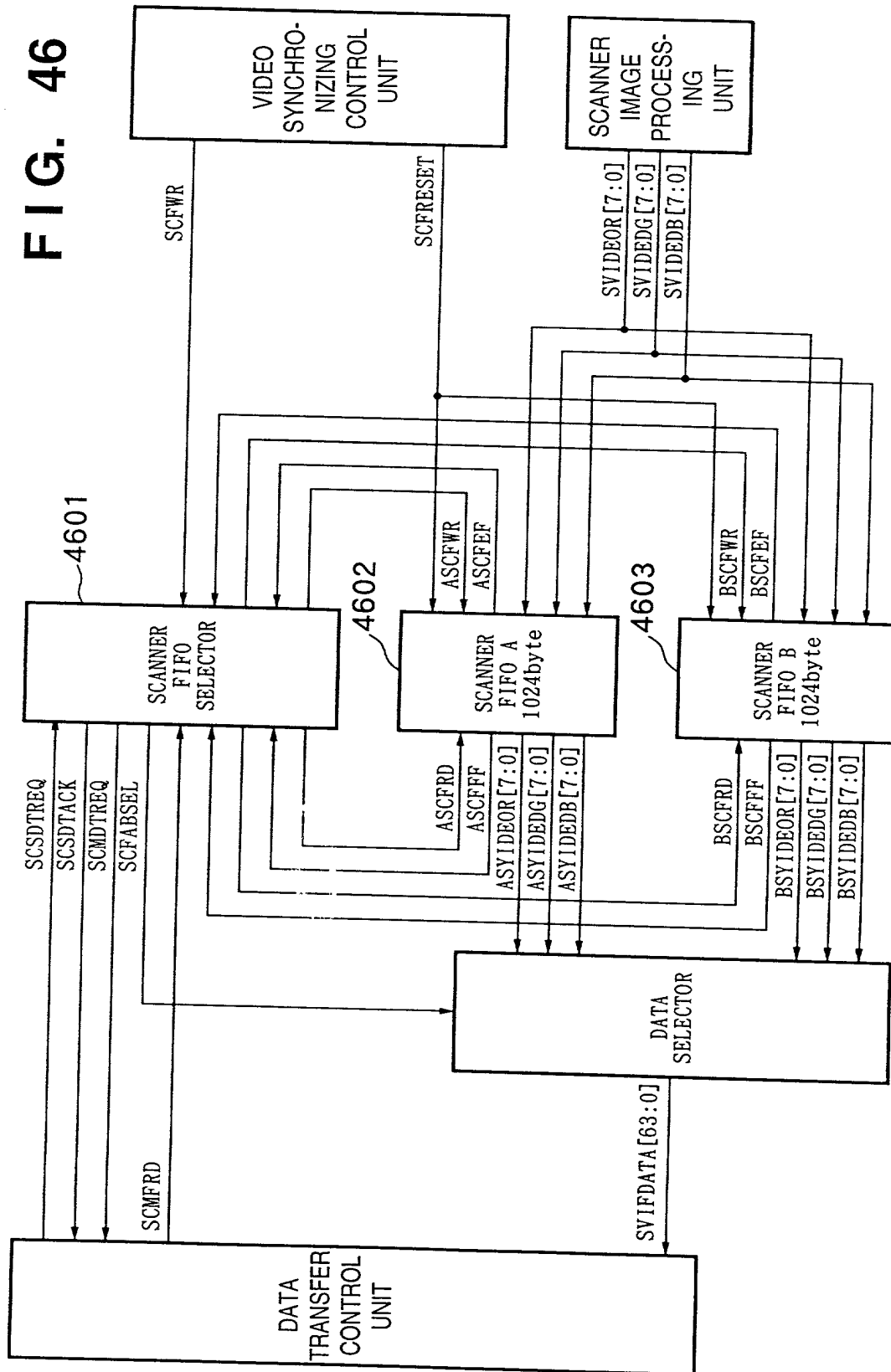


FIG. 45

FIG. 46



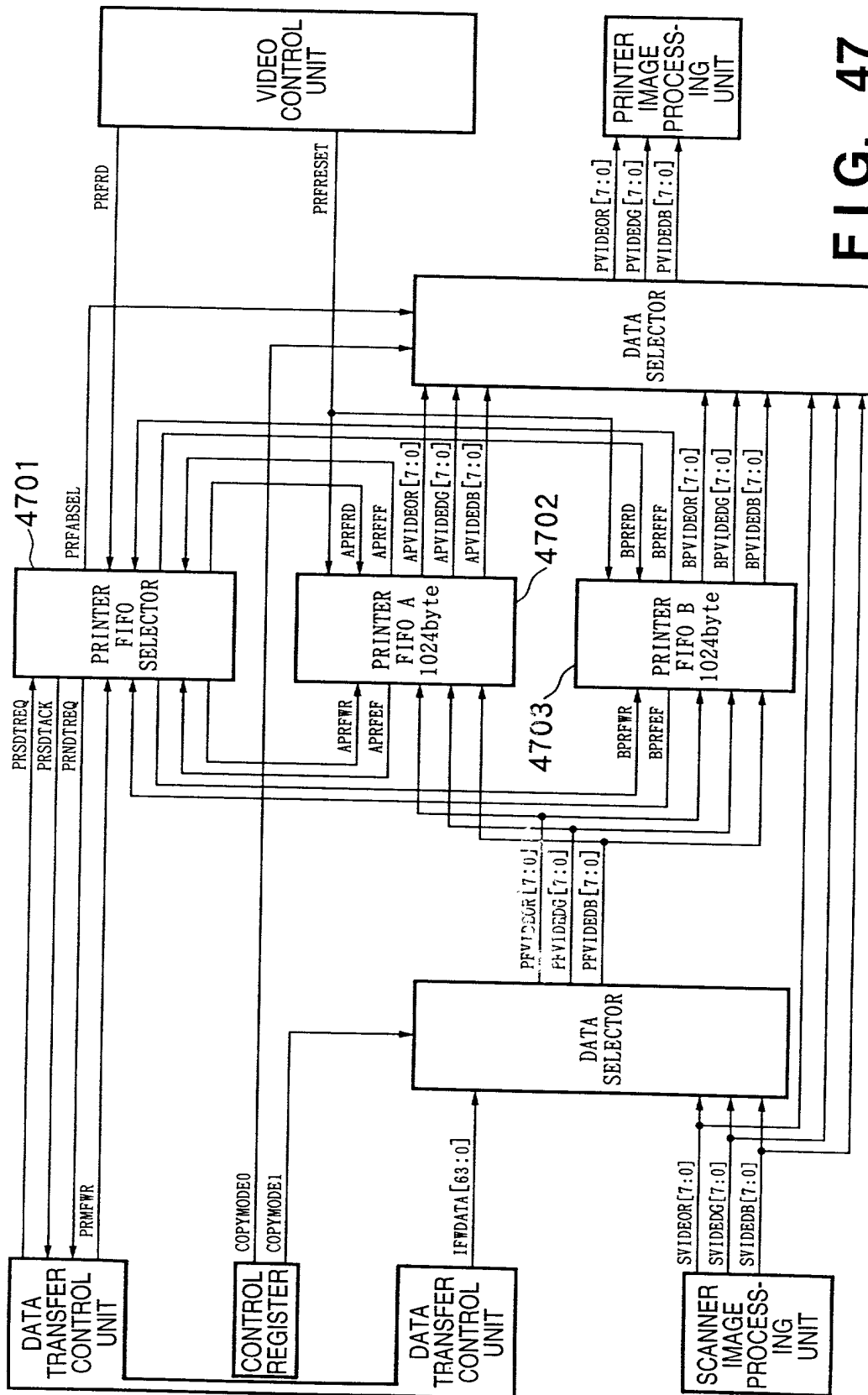
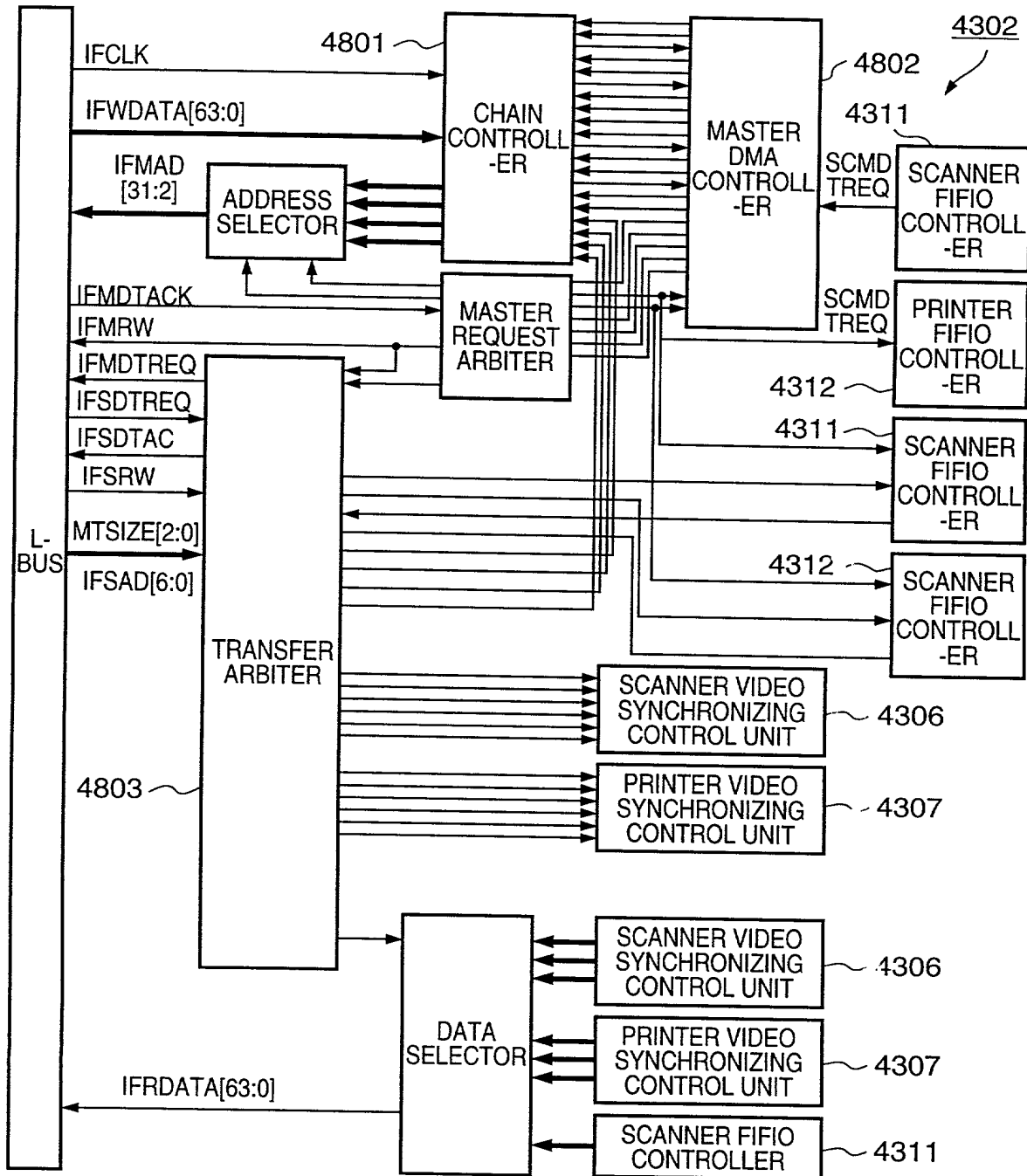


FIG. 47



FIG. 48



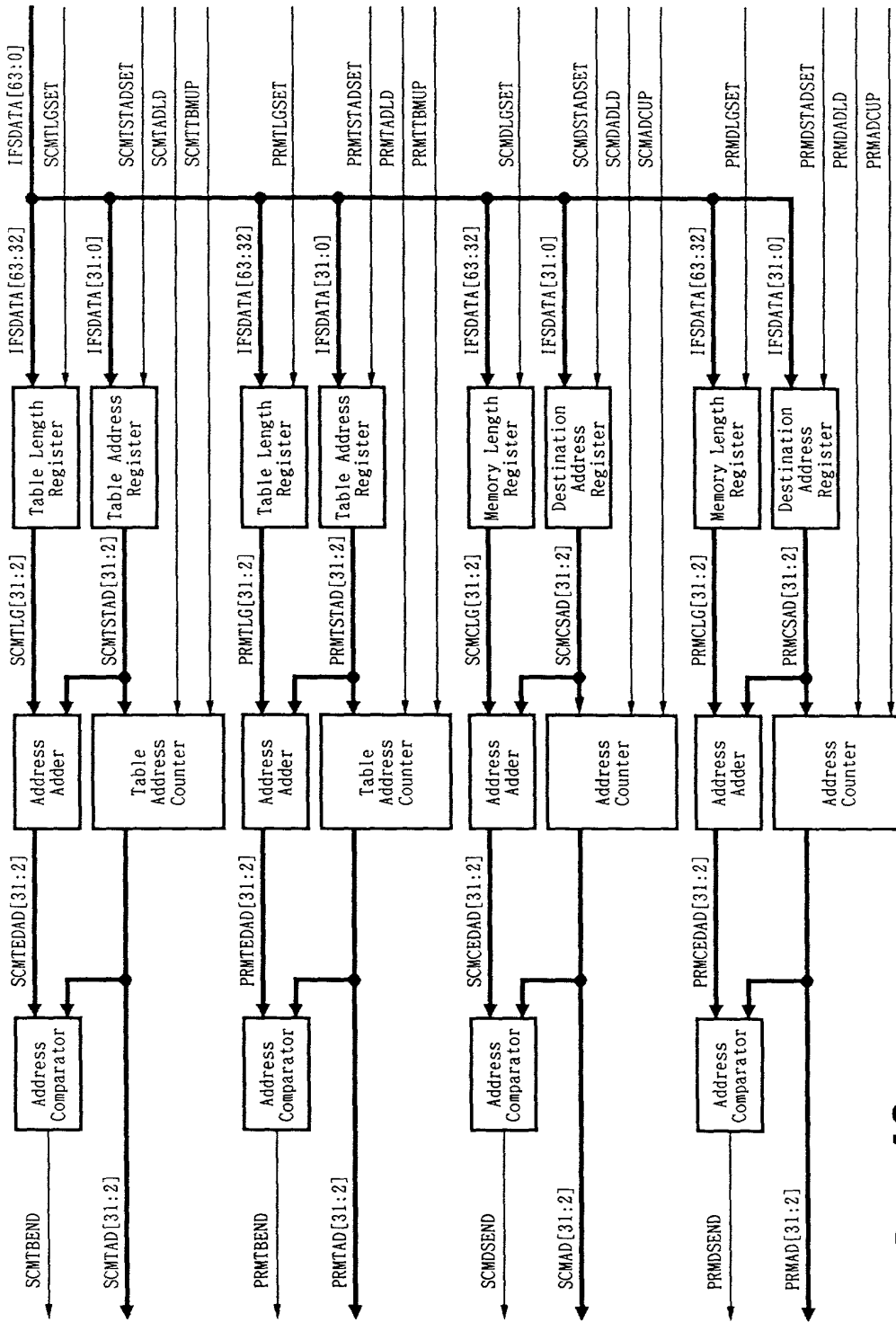


FIG. 49

FIG. 50

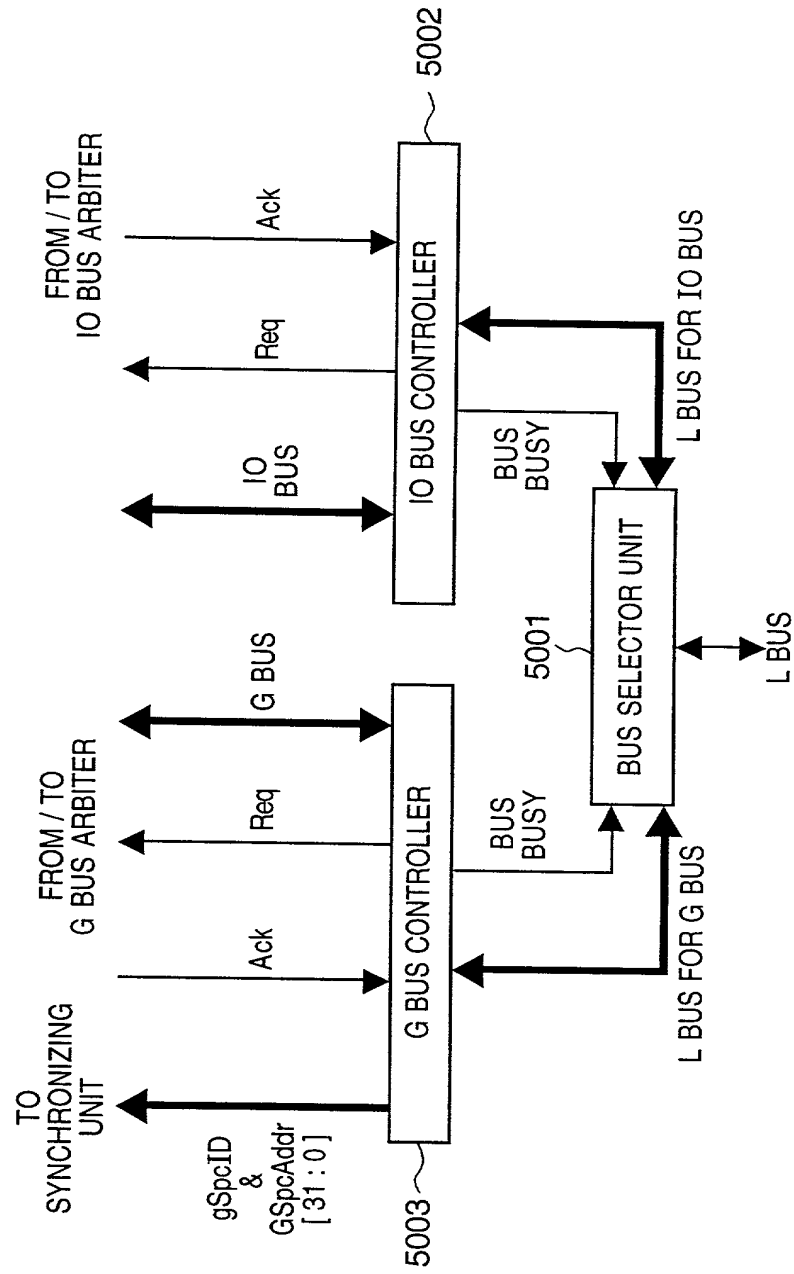
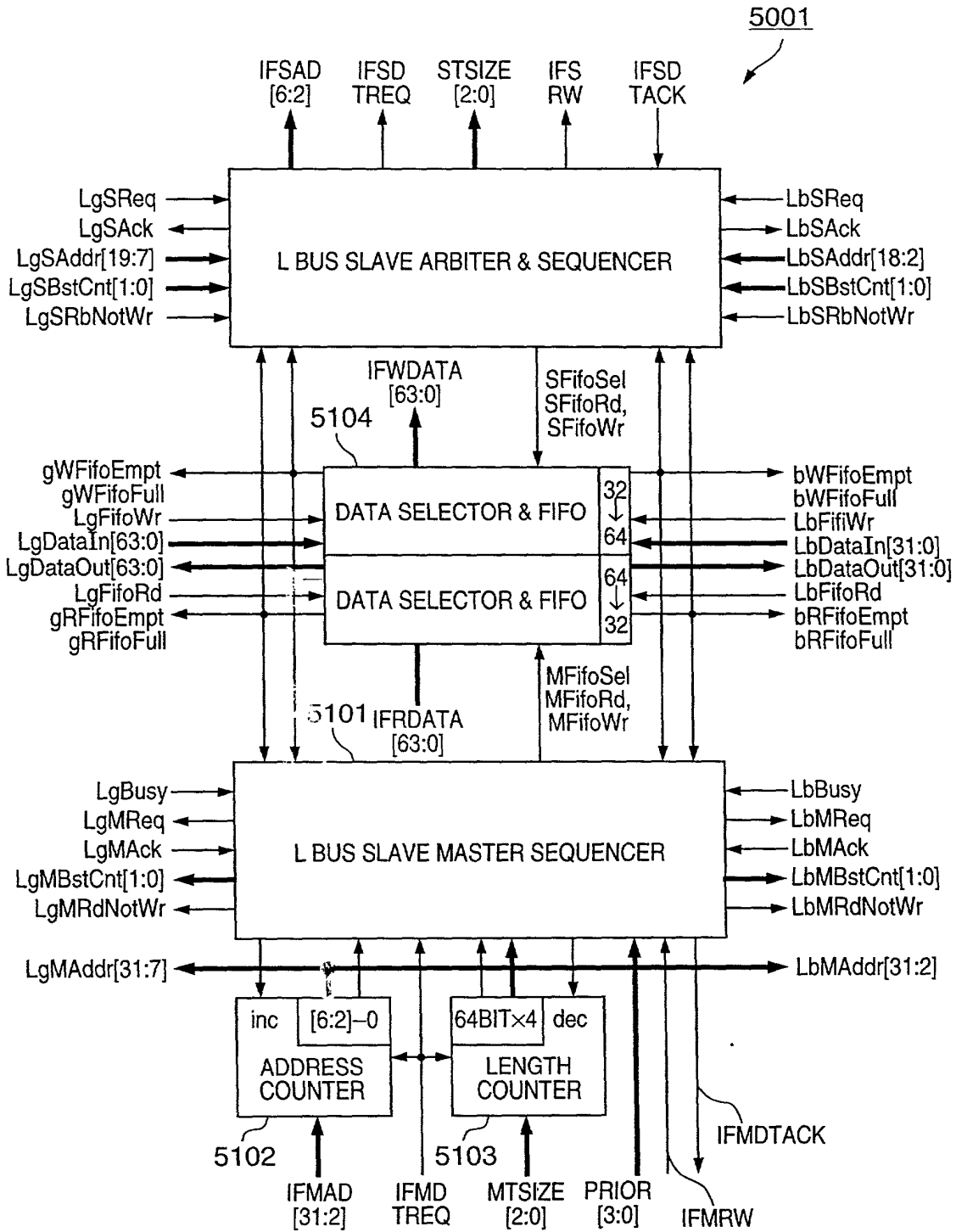


FIG. 51



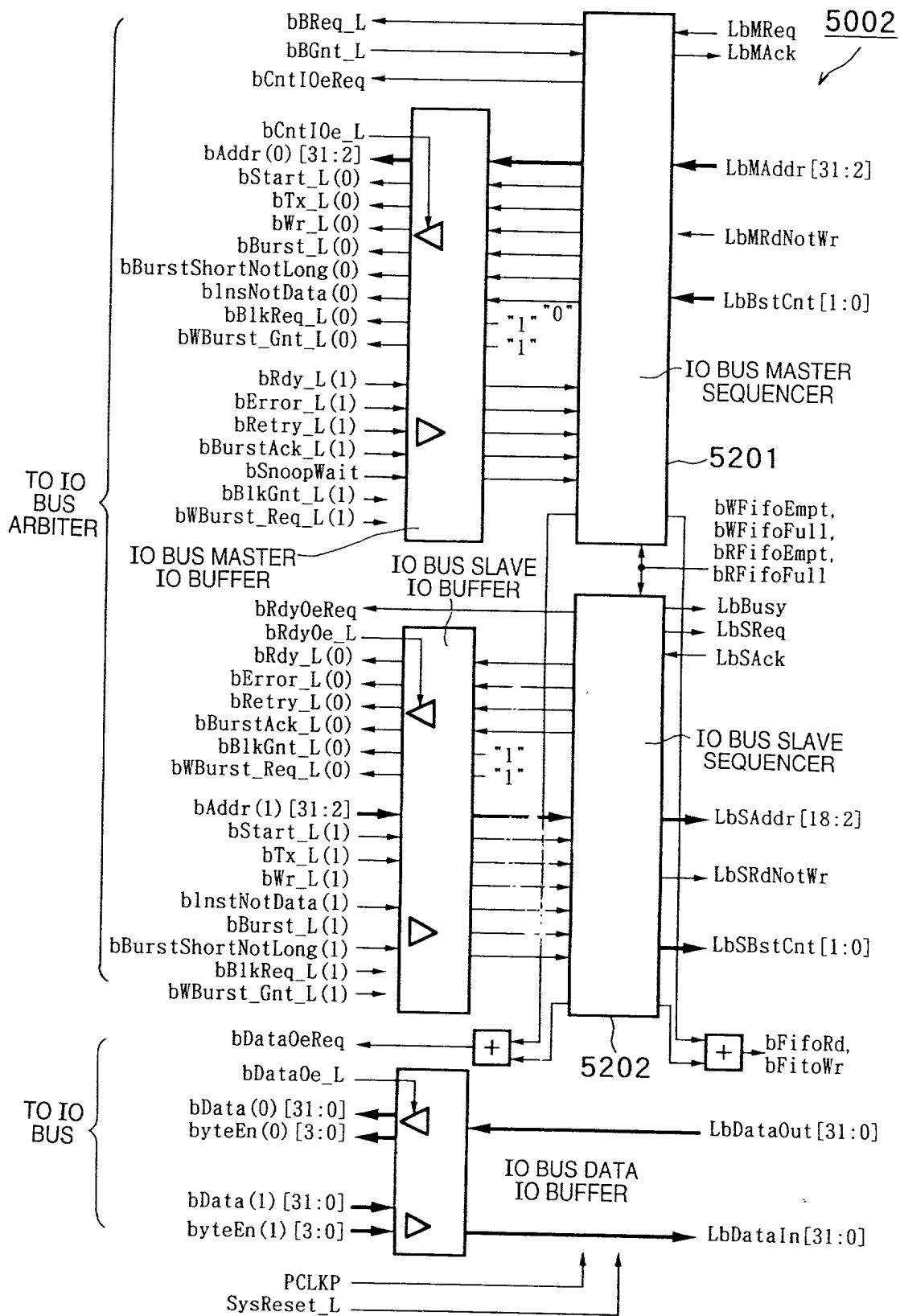


FIG. 52

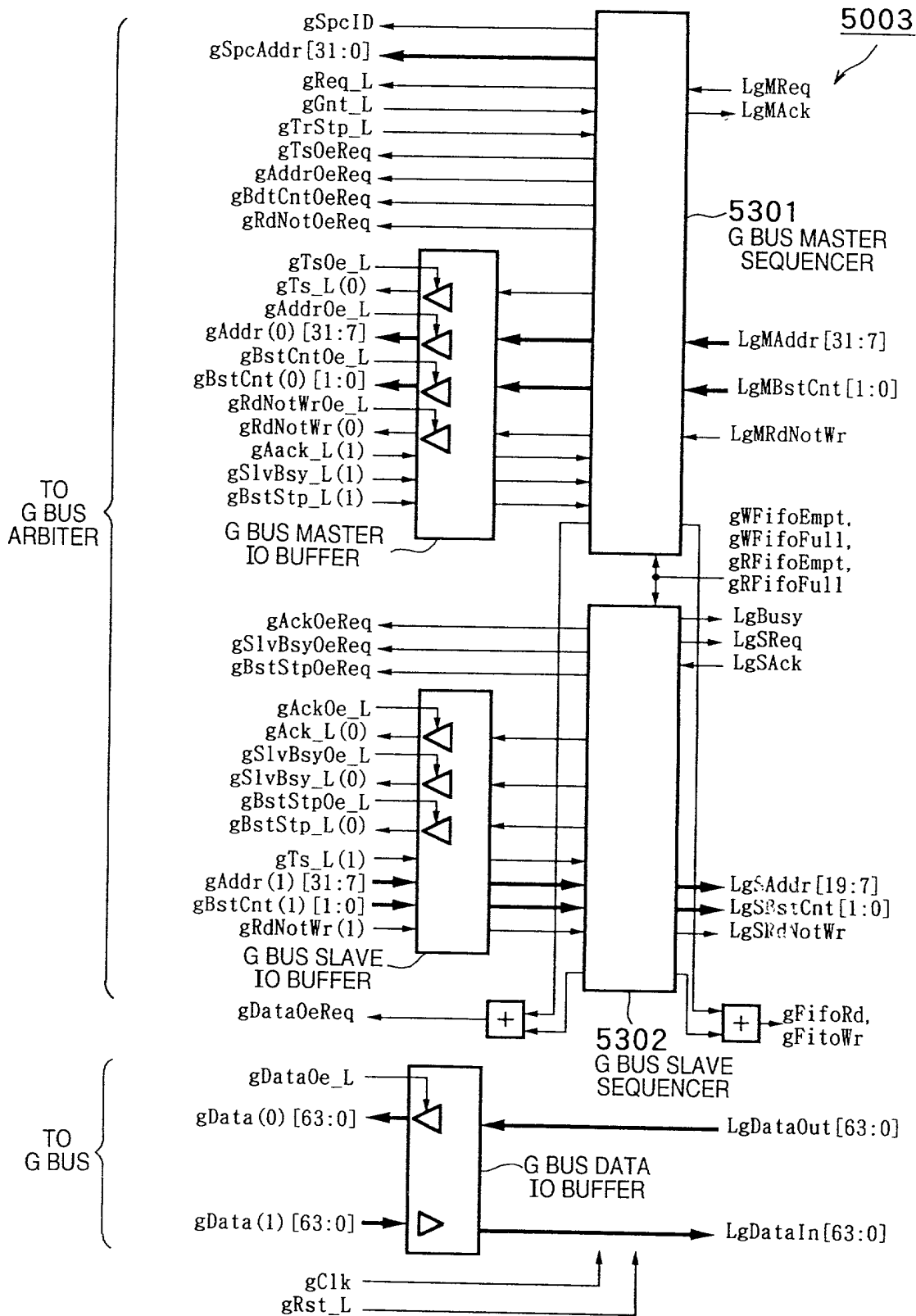


FIG. 53

FIG. 54

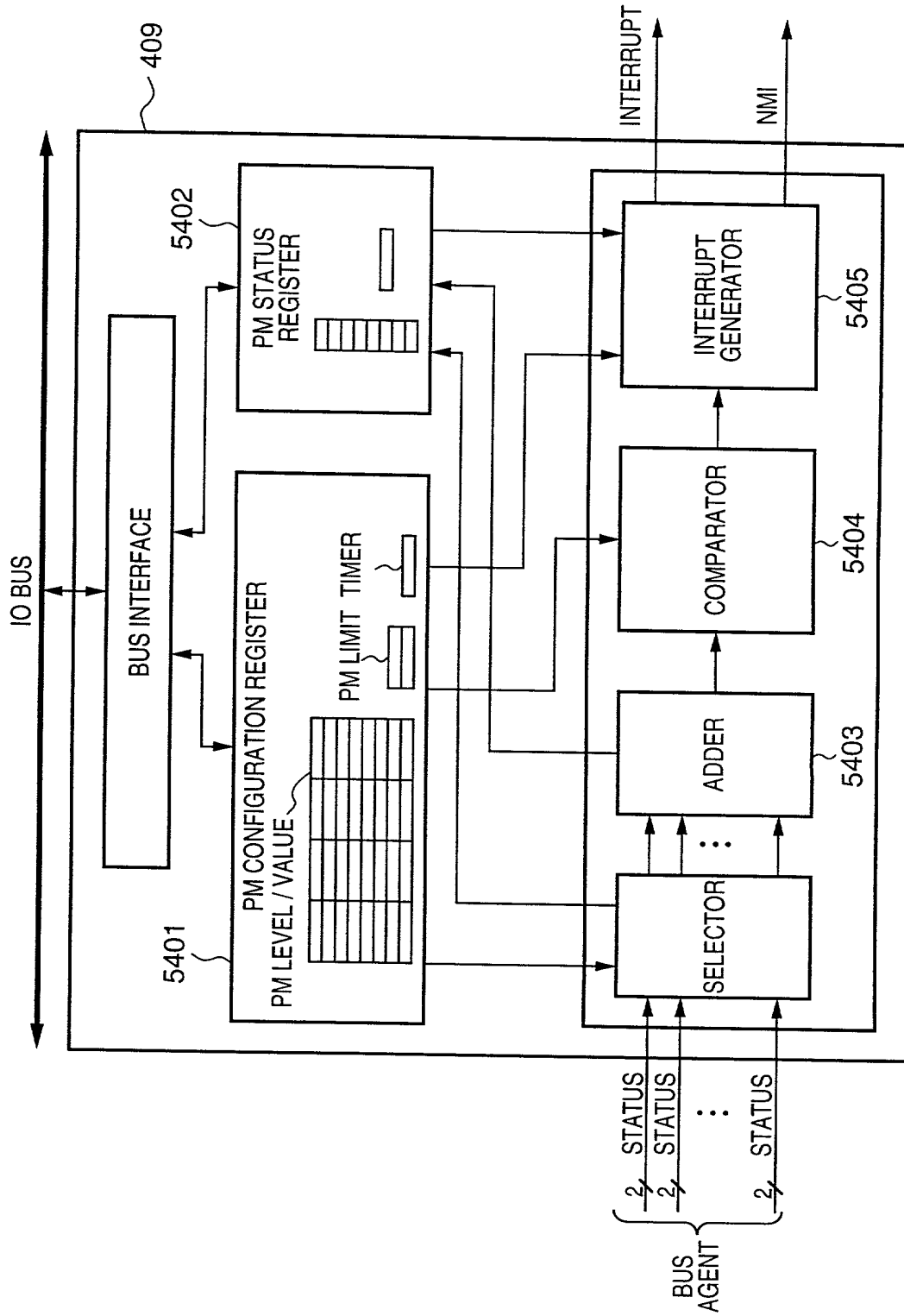
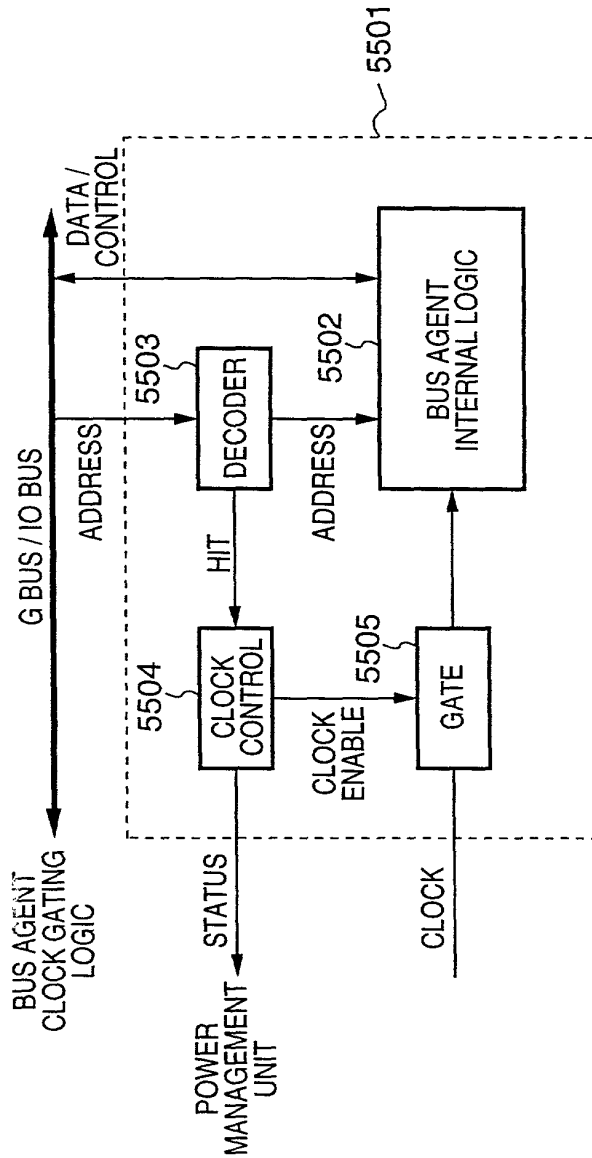


FIG. 55

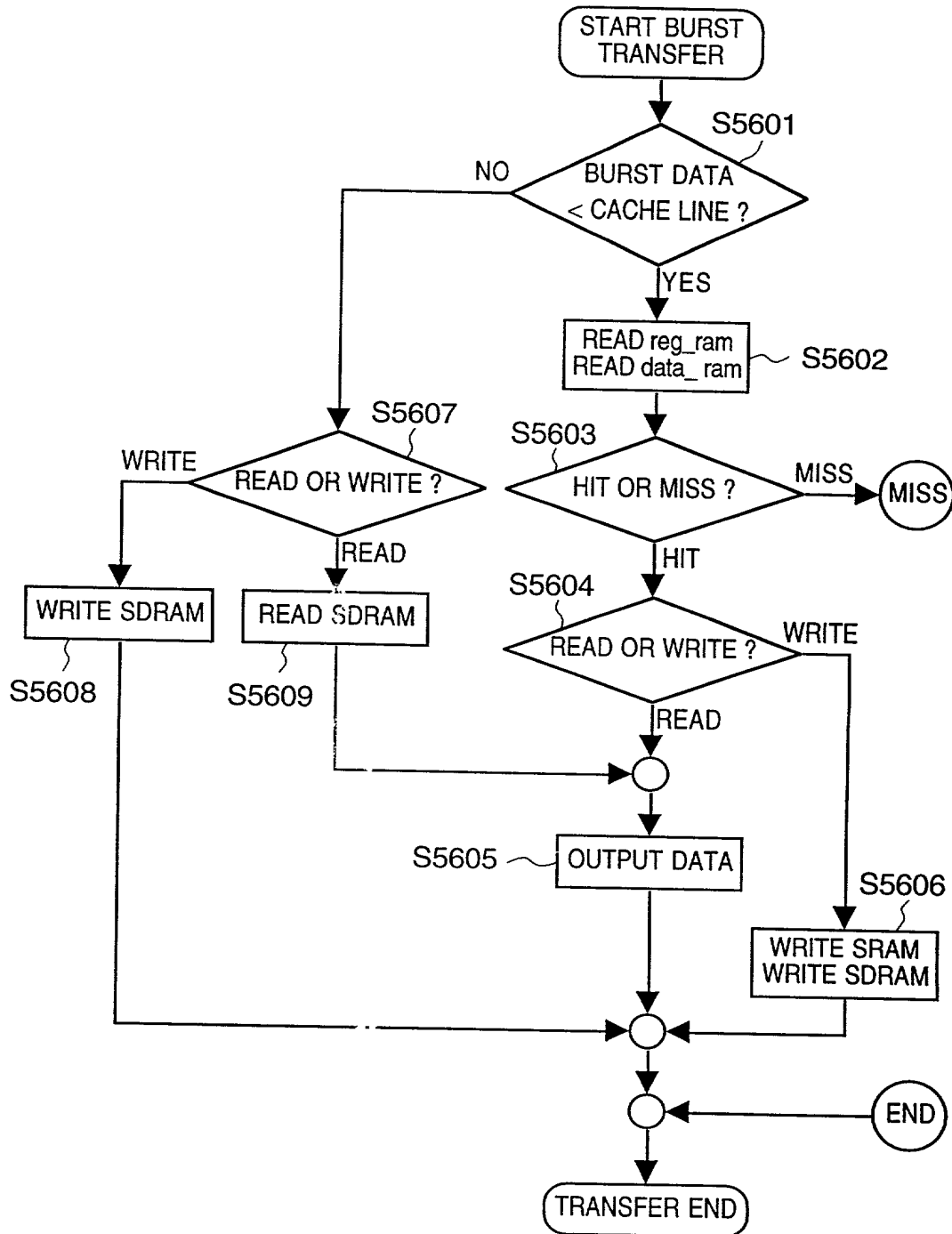


(CLOCK CONTROL)

- BUS AGENT DETECTS BUS ACTIVITY AND TURNS CLOCK ON AND OFF AUTOMATICALLY.
- THREE STATUS, NAMELY "SLEEP", "WAKE-UP" AND "WAIT".
- "SLEEP" IS A STATE IN WHICH BUS AGENT EXHIBITS NO ACTIVITY AND CLOCK HAS BEEN STOPPED.
- DECODER AND CLOCK CONTROLLER OPERATE EVEN IN SLEEP STATE; THEY MONITOR BUS AND WAIT FOR REQUEST.
- WHEN DECODER DETECTS ITS OWN ADDRESS, IT OPENS CLOCK GATE, ACTIVATES CLOCK OF INTERNAL LOGIC IS ACTIVATED AND COMPLIES WITH BUS REQUEST. STATE SHIFTS TO WAKE-UP.
- WHEN DATA TRANSFER ENDS, TRANSITION IS MADE TO WAIT STATE AND NEXT REQUEST IS AWAITED. CLOCK REMAINS ACTIVE. IF THERE IS REQUEST, WAKE-UP STATE IS RESTORED AND TRANSFER IS CARRIED OUT. COUNTING IS PERFORMED BY TIMER WHILE REQUEST IS BEING AWAITED.
- IF TIMER RUNS OUT OR TIME WITHOUT REQUEST BEING ISSUED, TRANSITION IS MADE TO SLEEP STATE AND CLOCK IS STOPPED.



FIG. 56



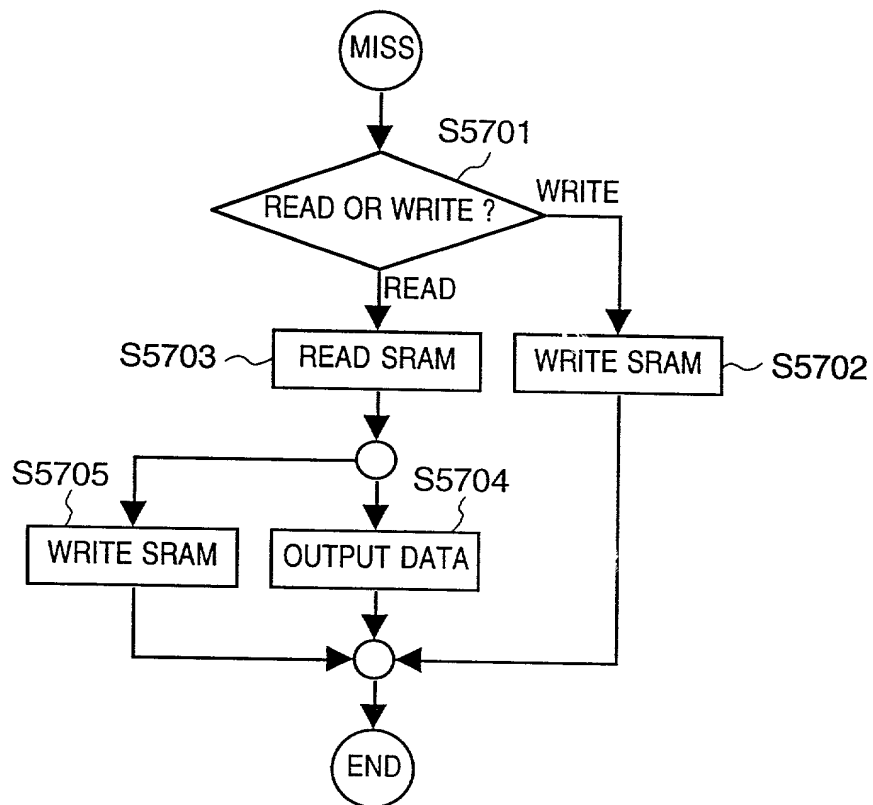
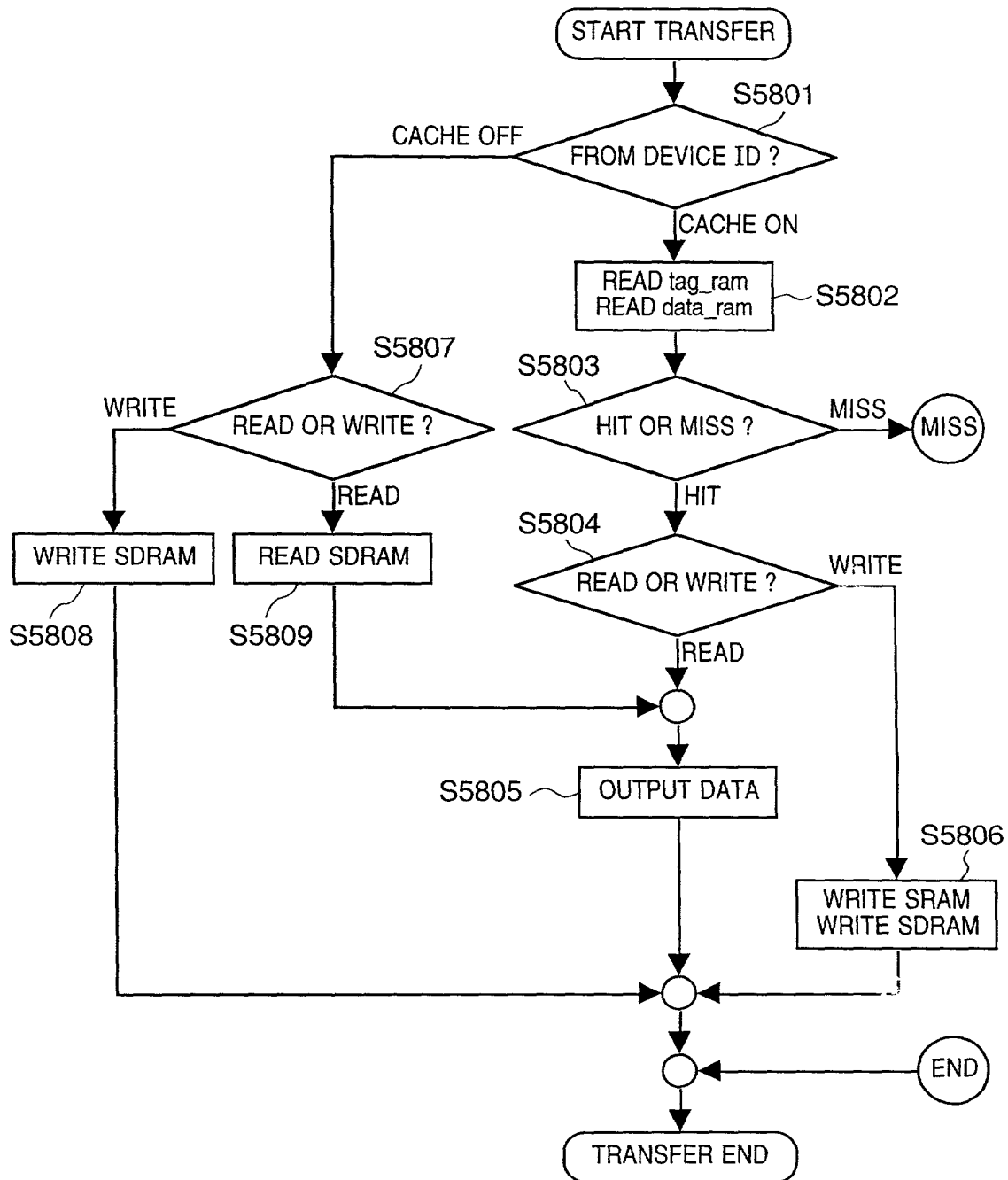
**FIG. 57**

FIG. 58



**F I G. 59**